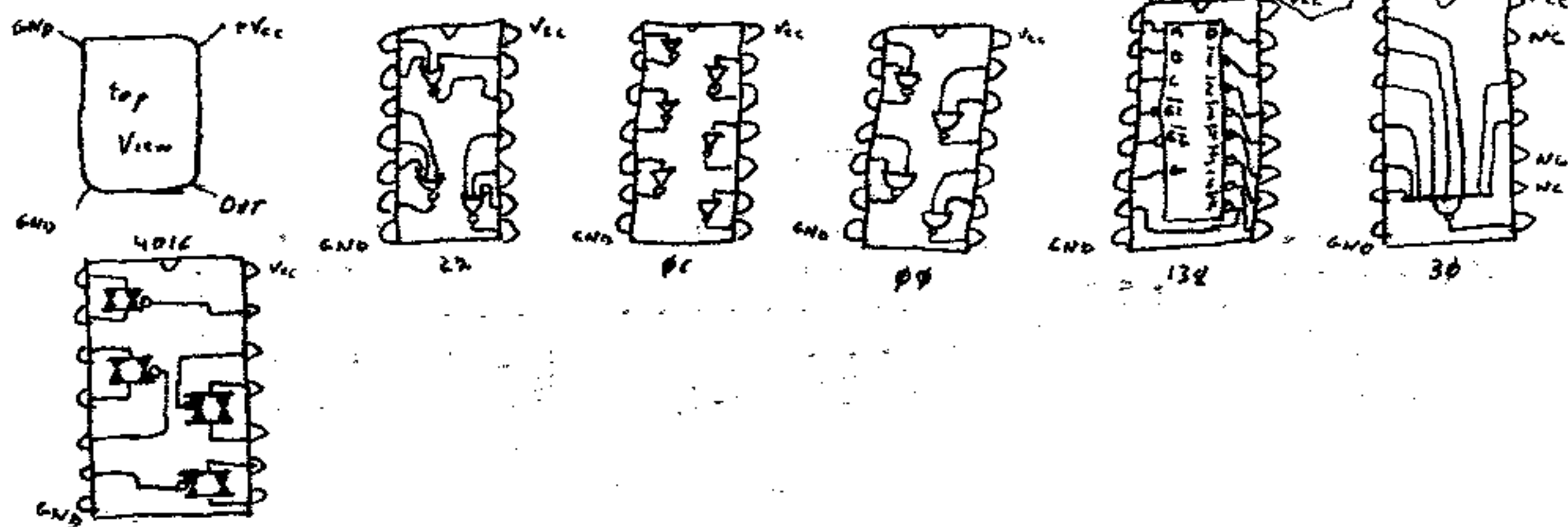
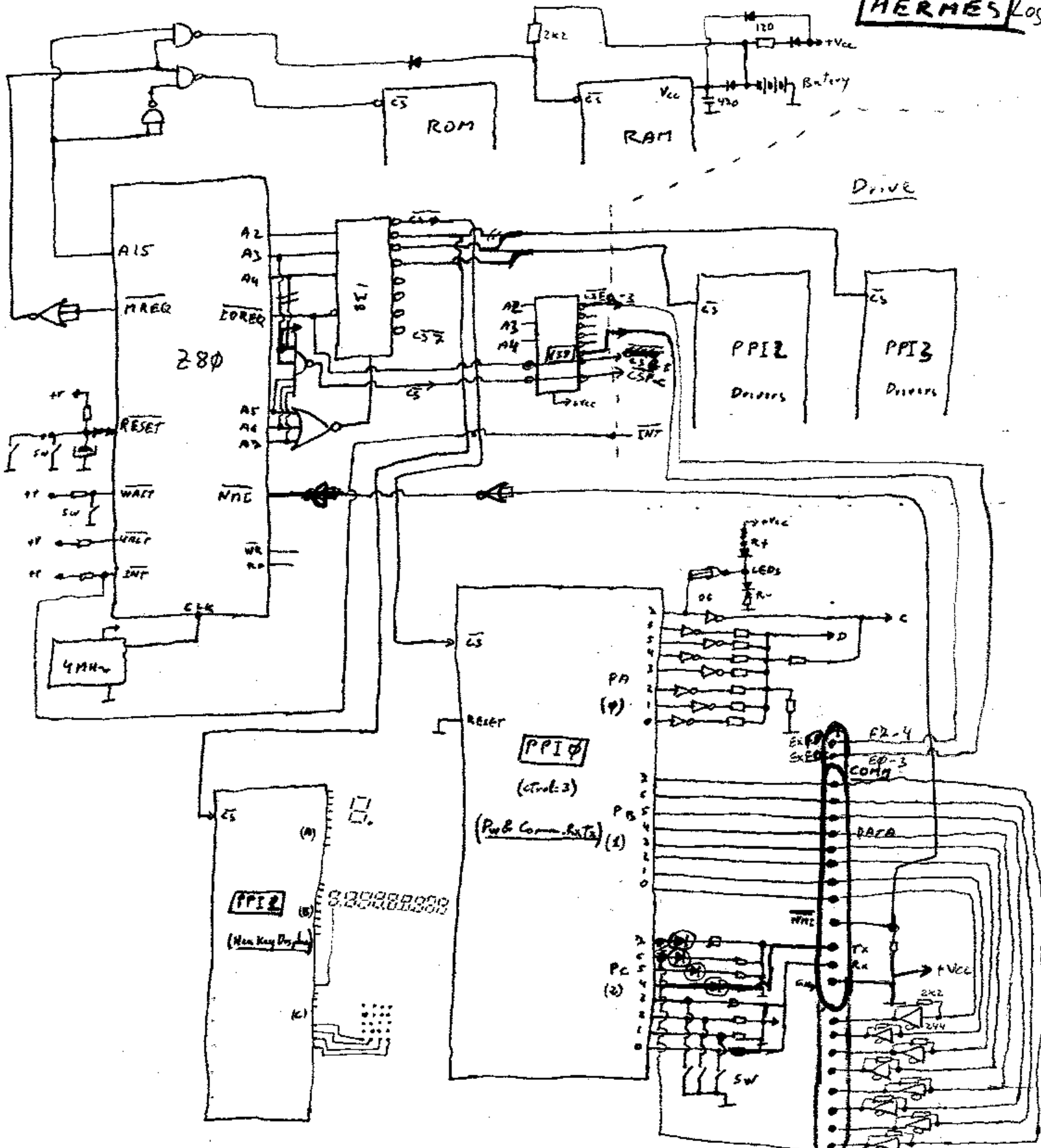
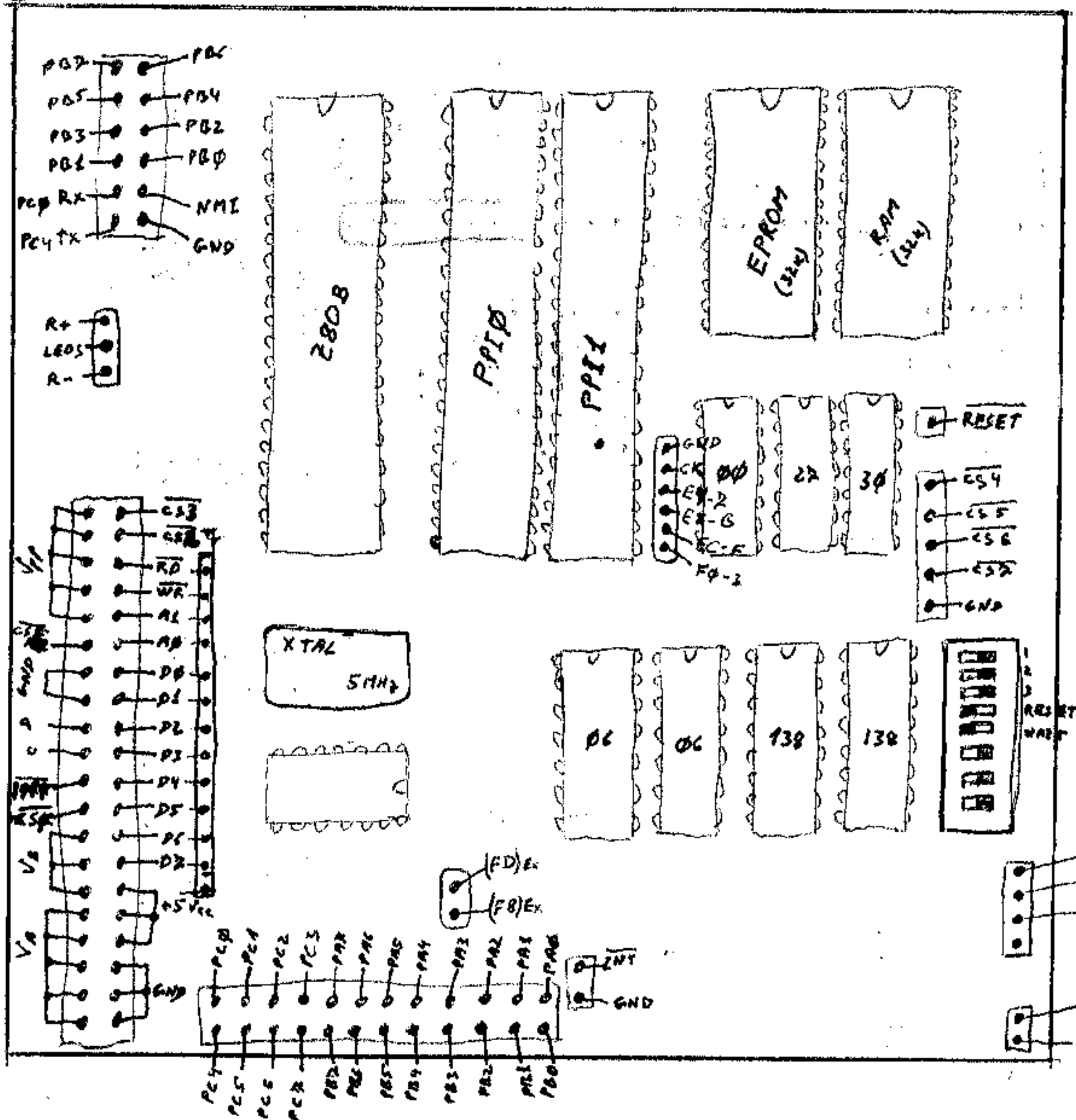
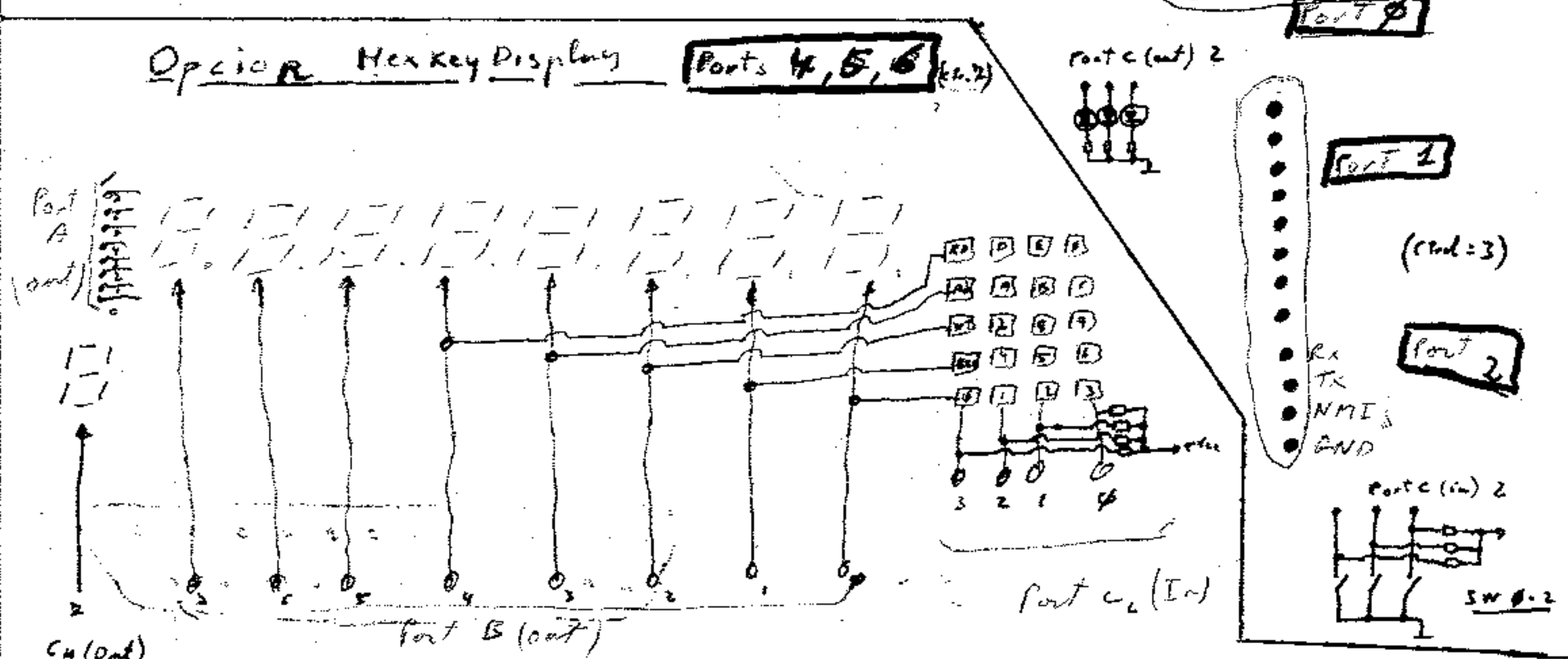




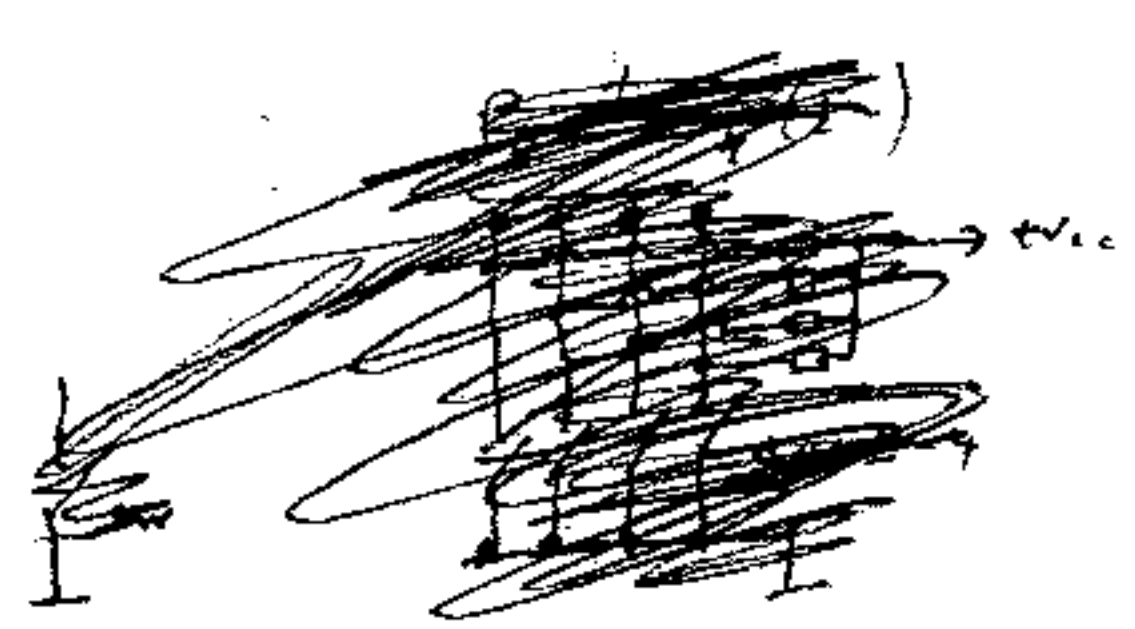
HERMES (CONTROL)



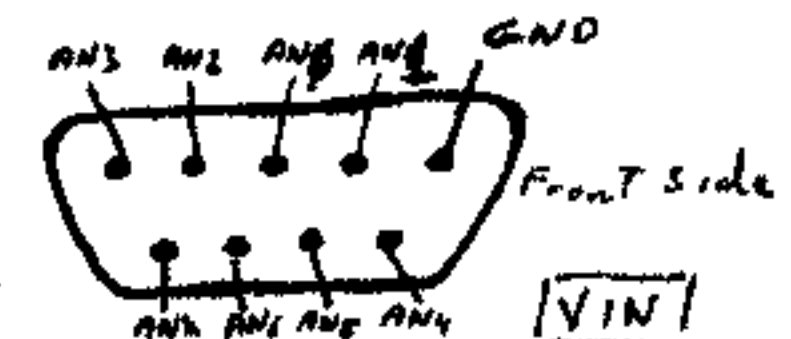
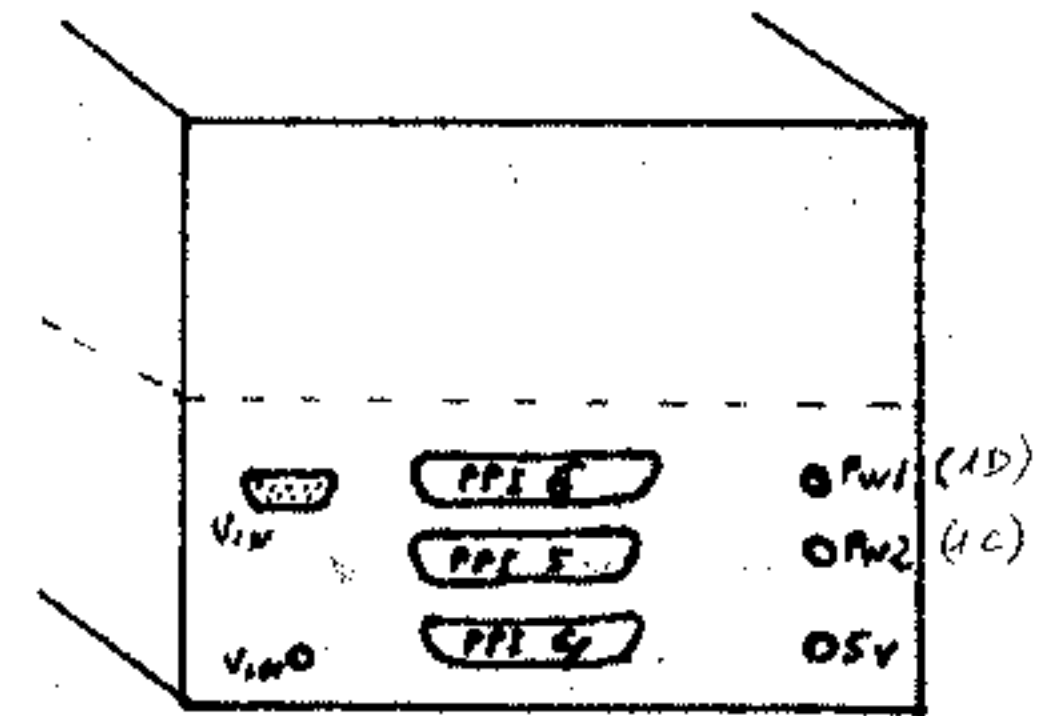
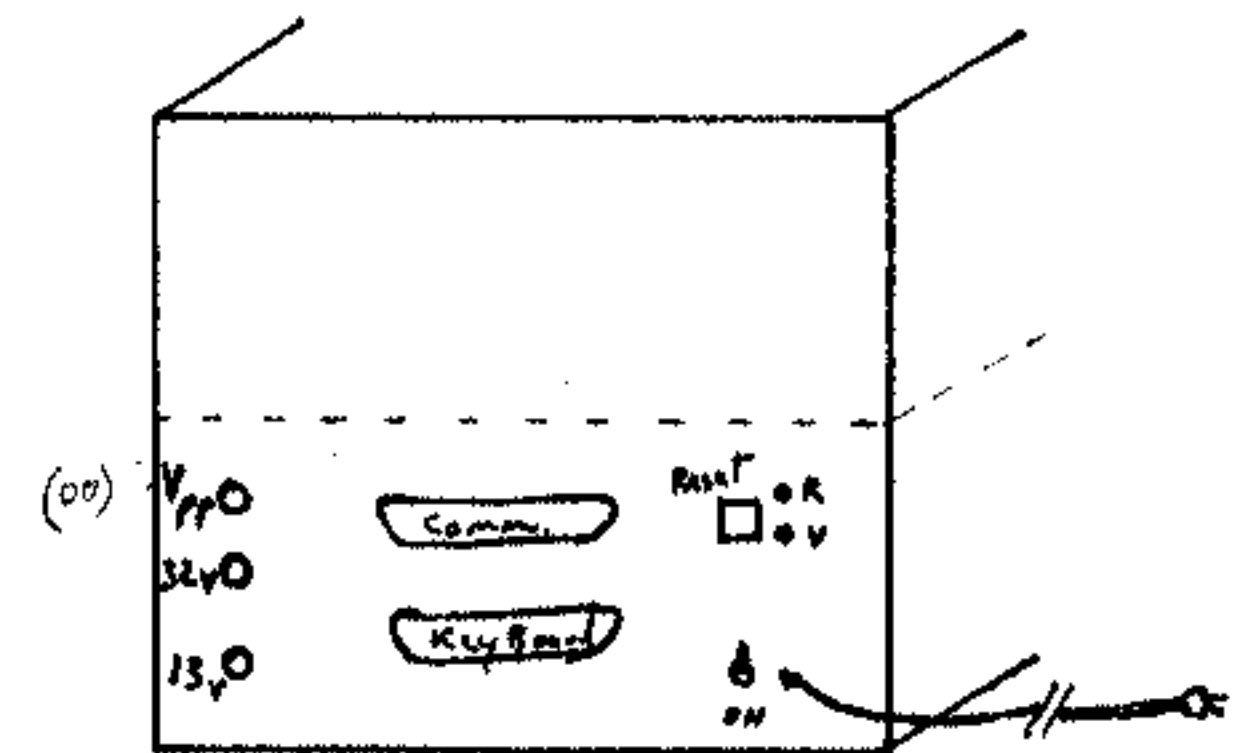
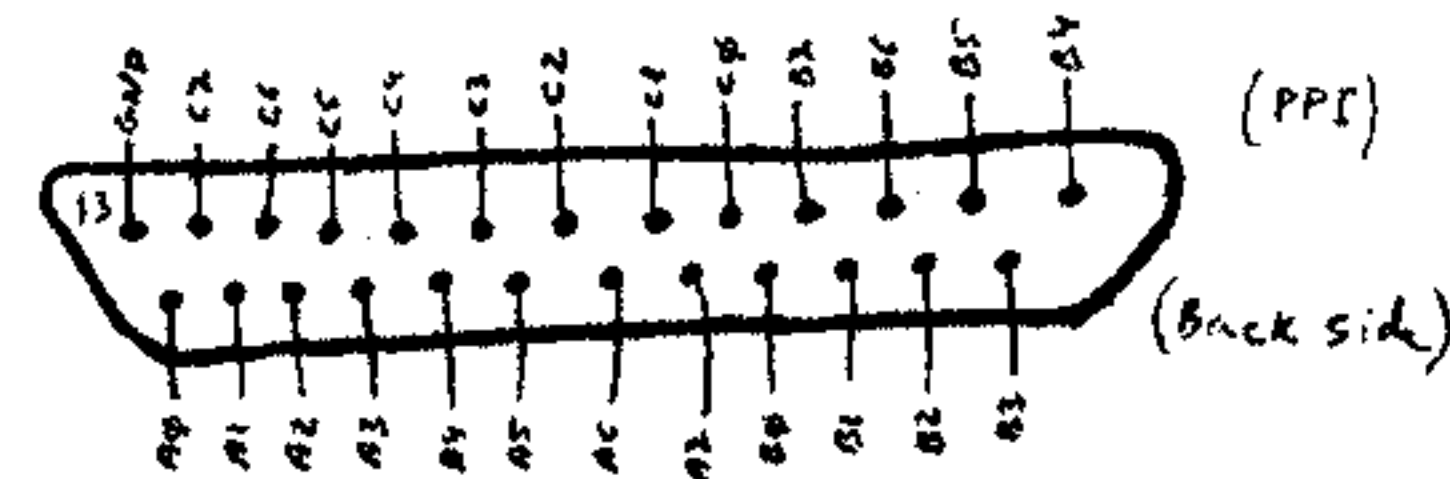
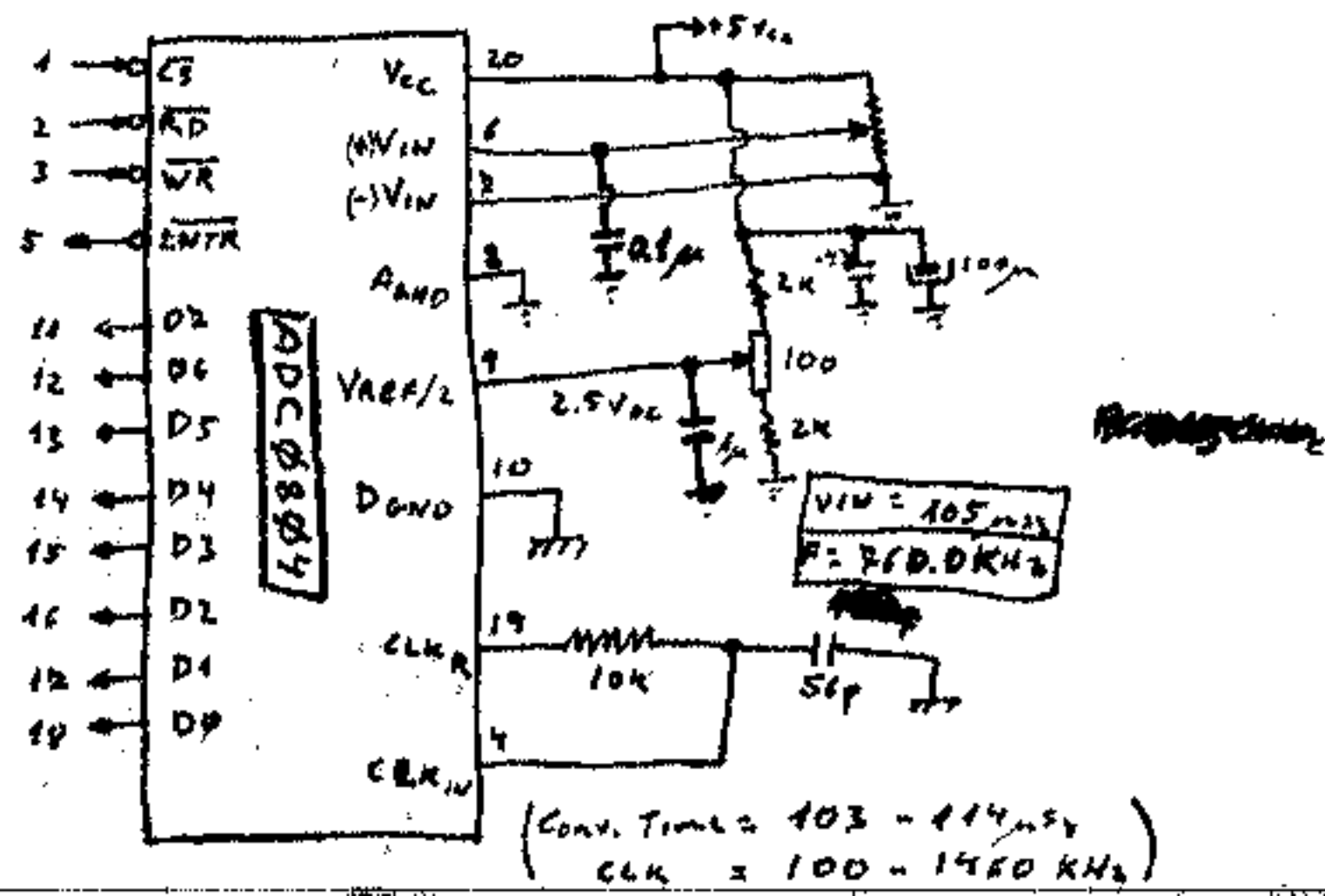
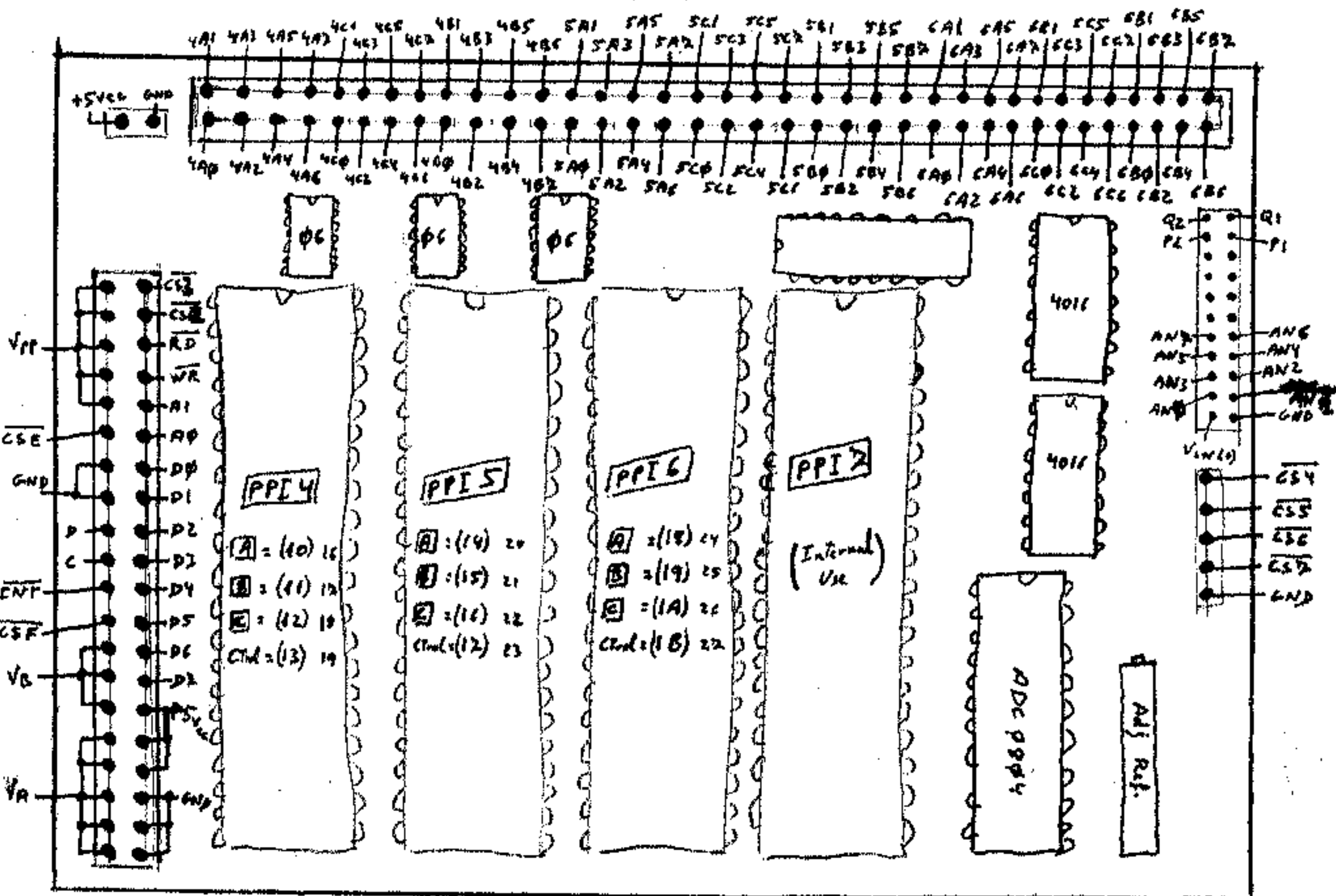
SW	@	add	
0	1112	045D	LEVEL 0 Diagnostics
1	1346	0542	CTROL KEYS
2	1624	0658	Hex. Programming
3			DONISOS
4			Command PGM
5			
6			
7			

[illegible]

EXTERNAL PORTS				
Port	(4)	(5)	(6)	(7)
A	16	20	24	28
B	12	21	25	29
C	18	22	26	30
D	19	23	27	31



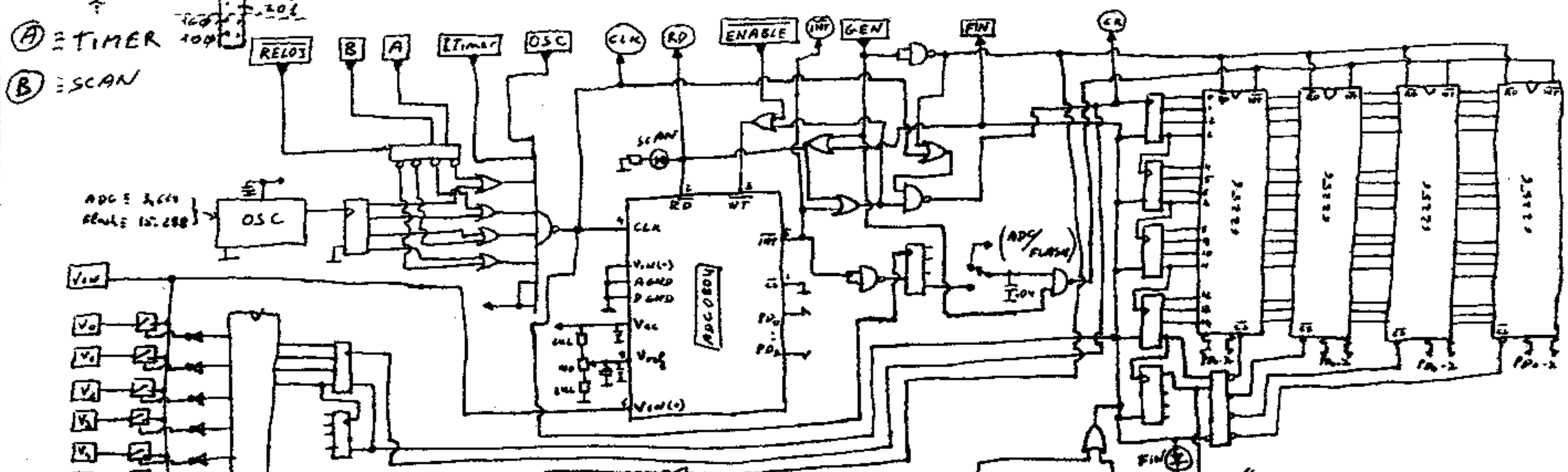
HERMES (Ports)



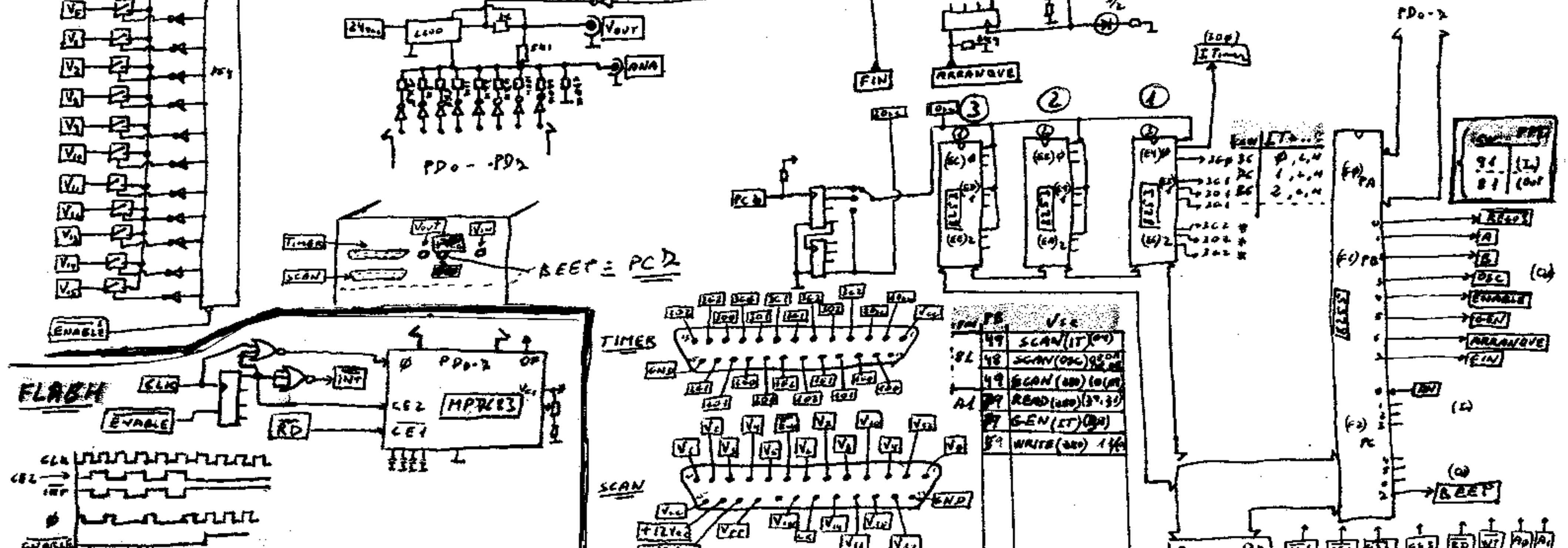
SCANNER & WAVE GENERATOR

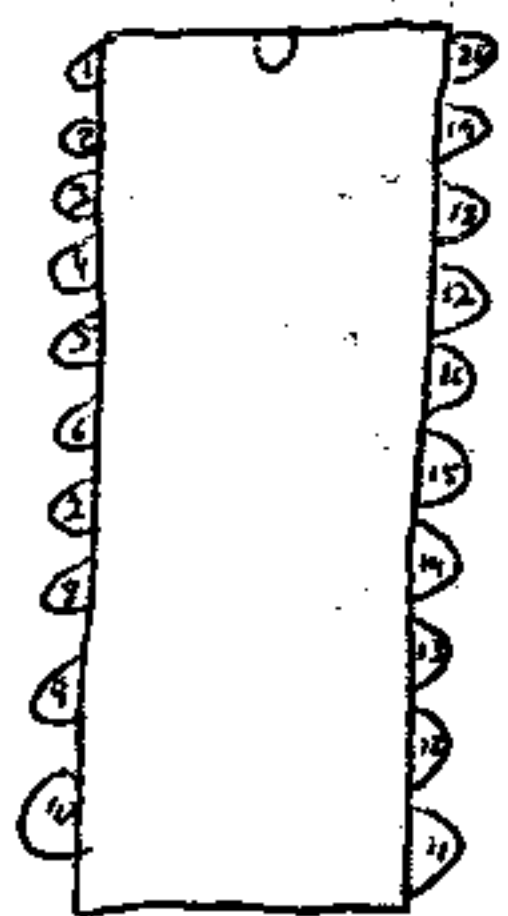
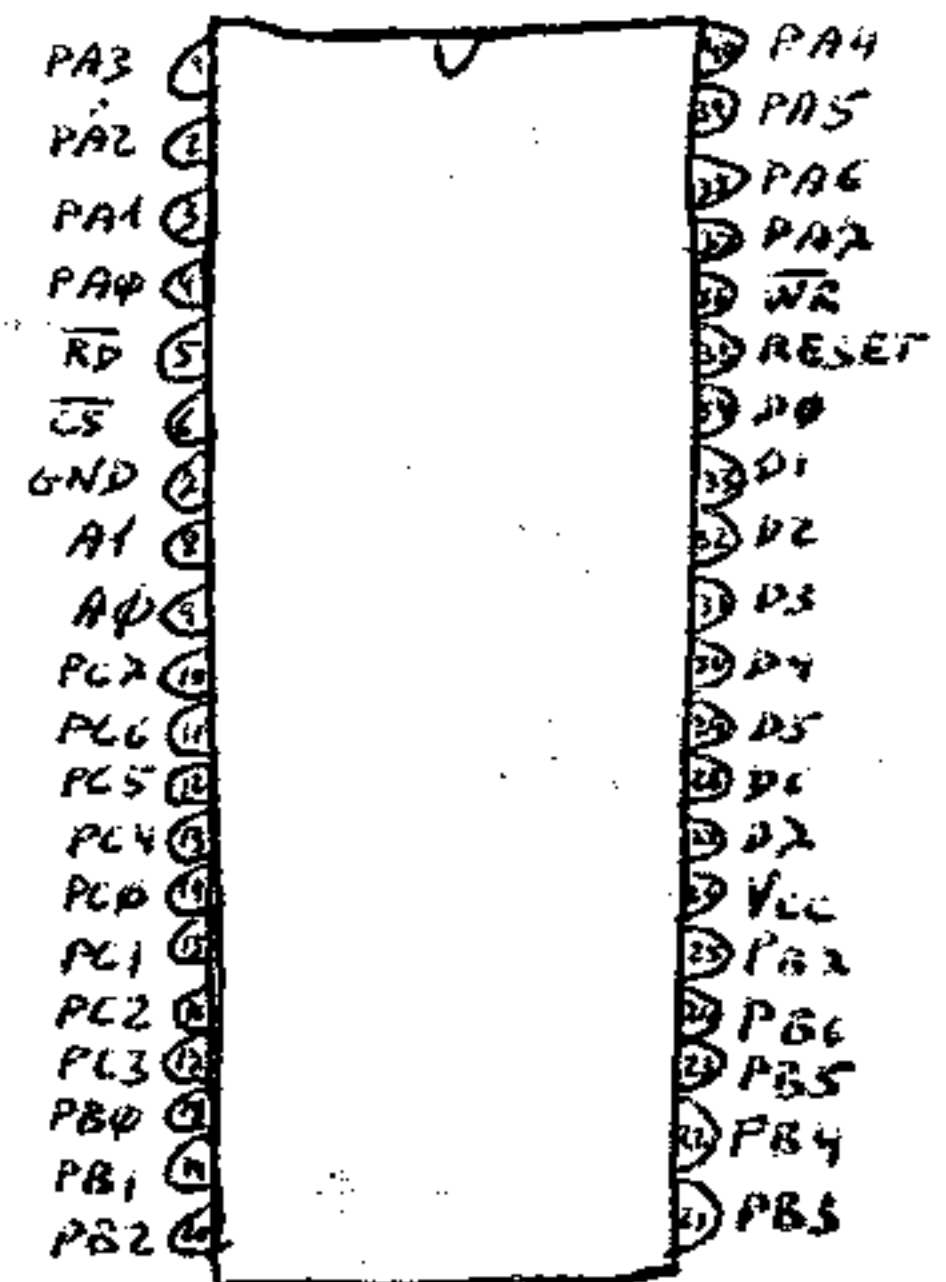
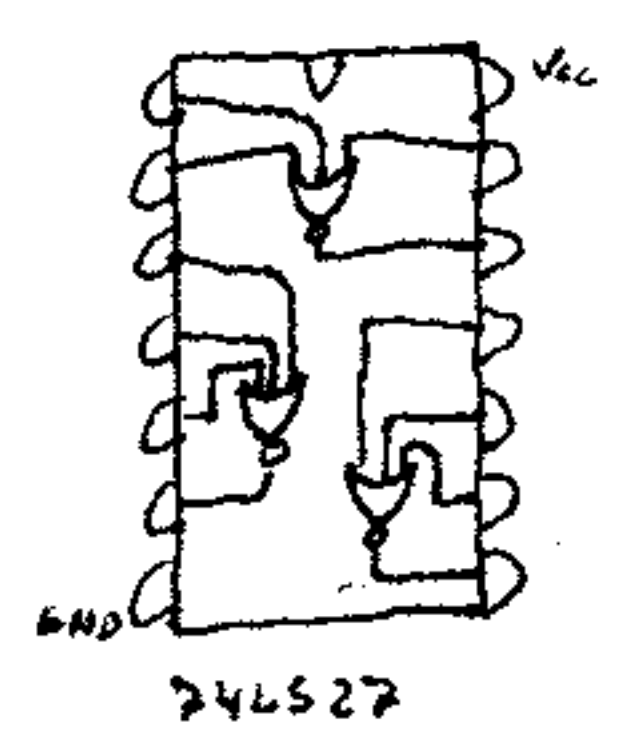
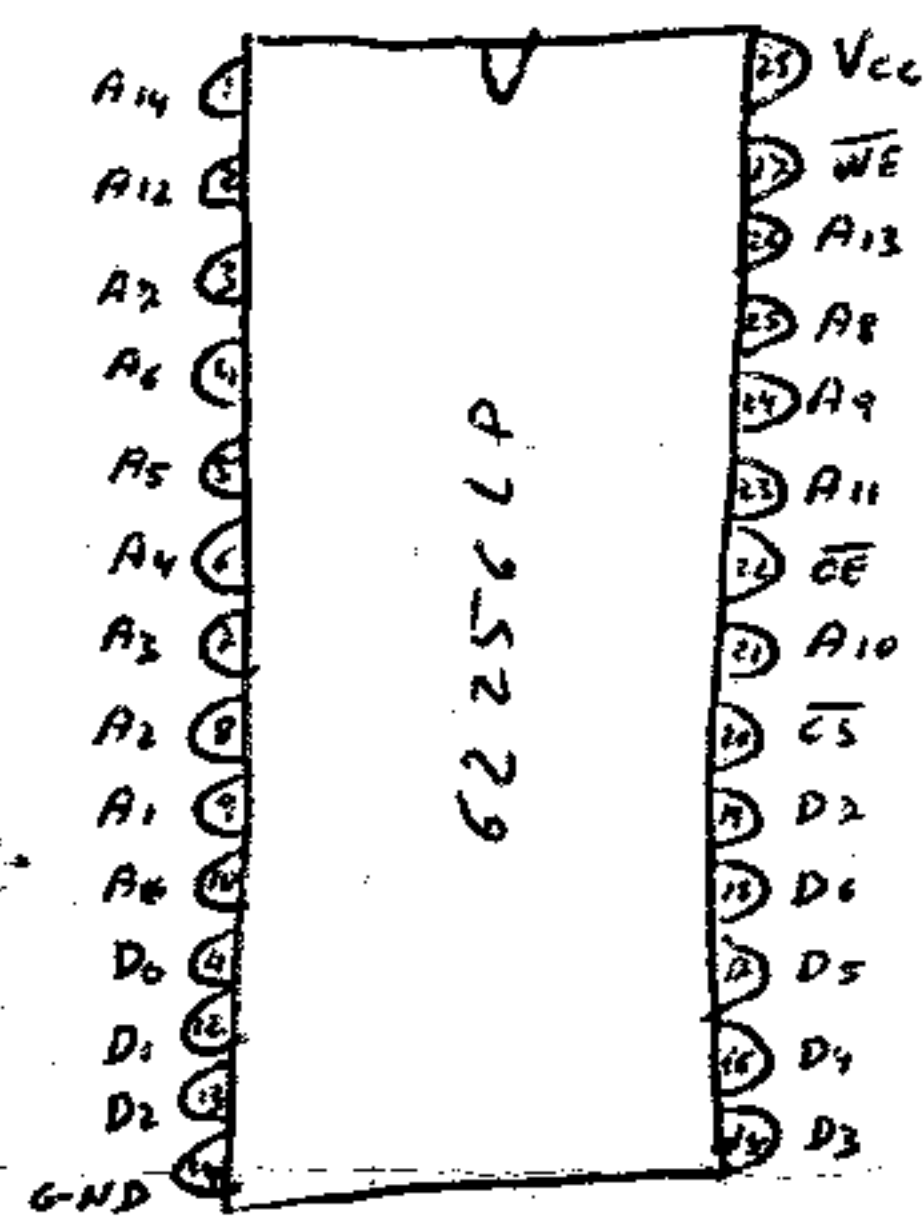
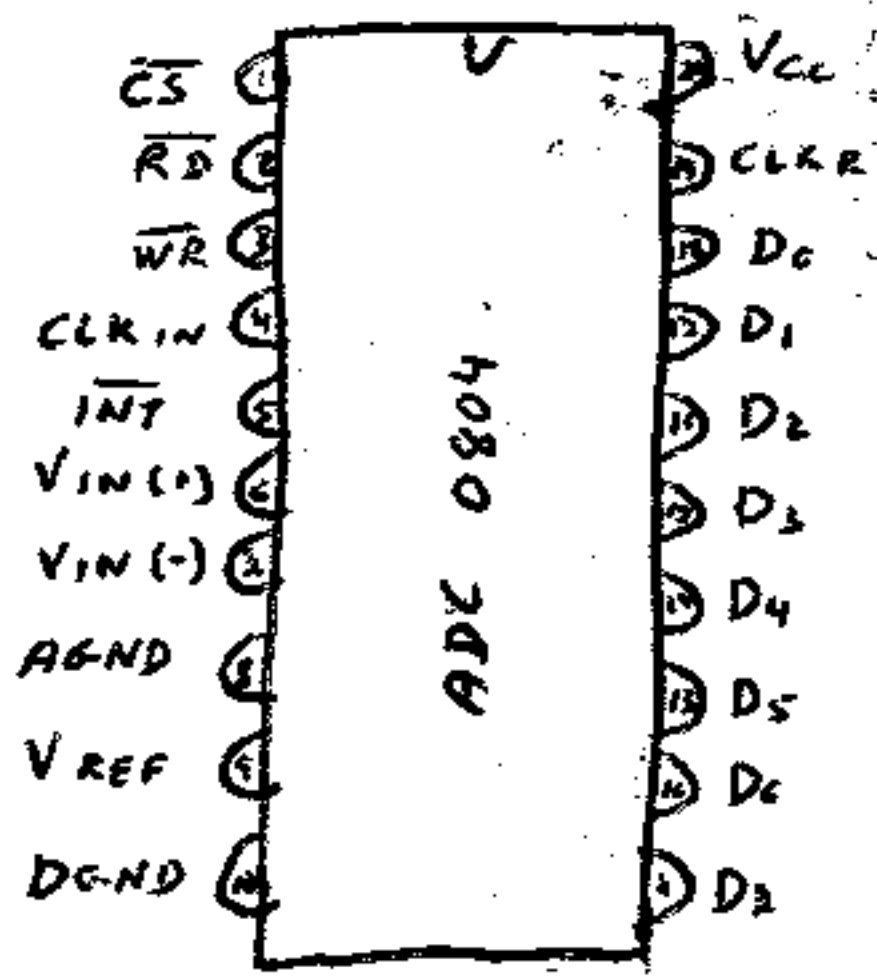
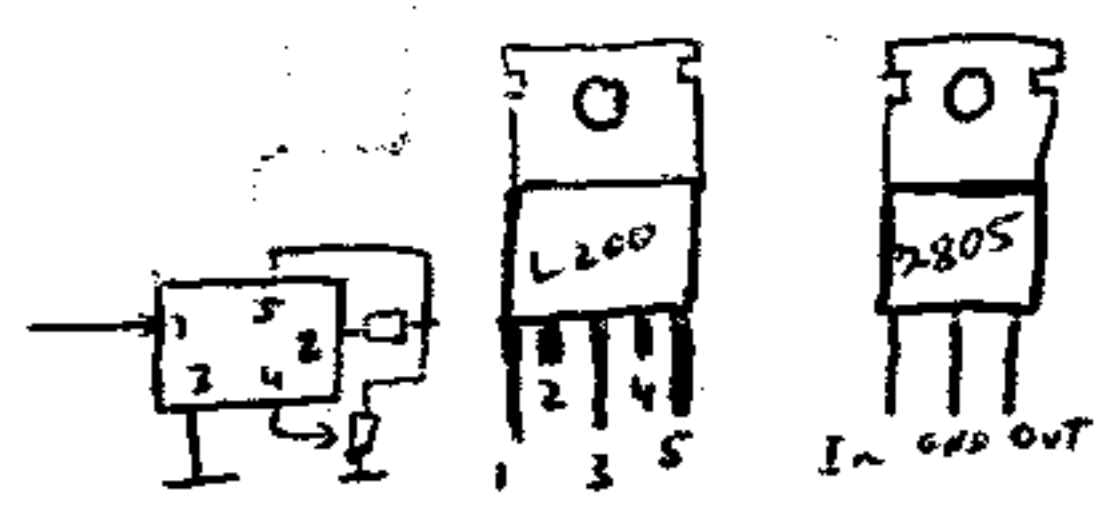
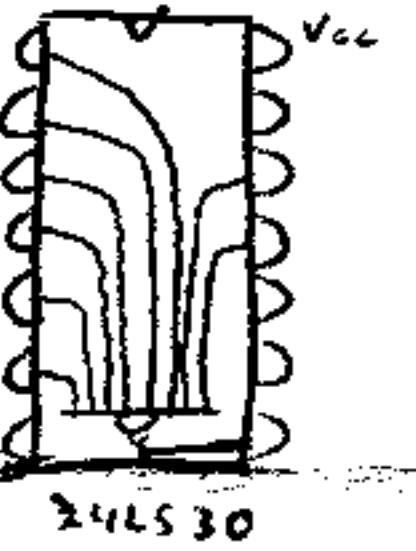
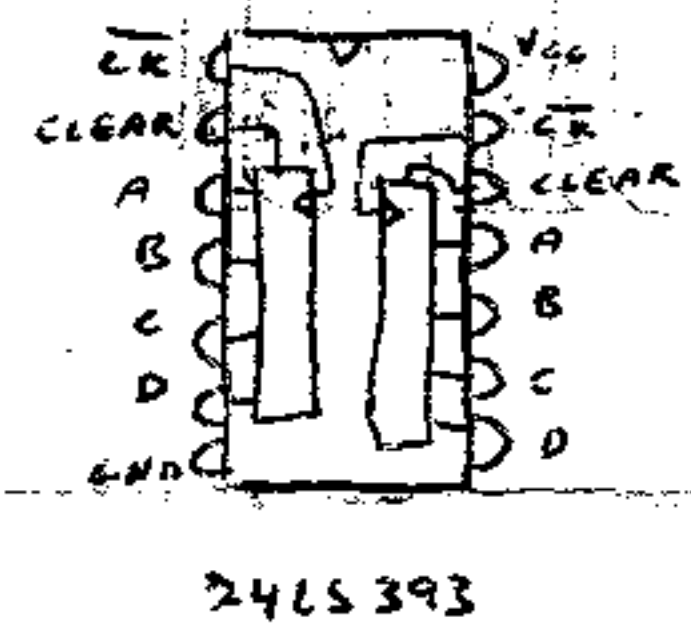
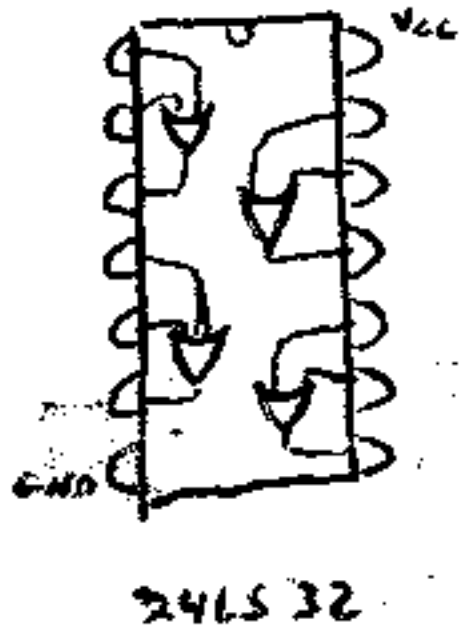
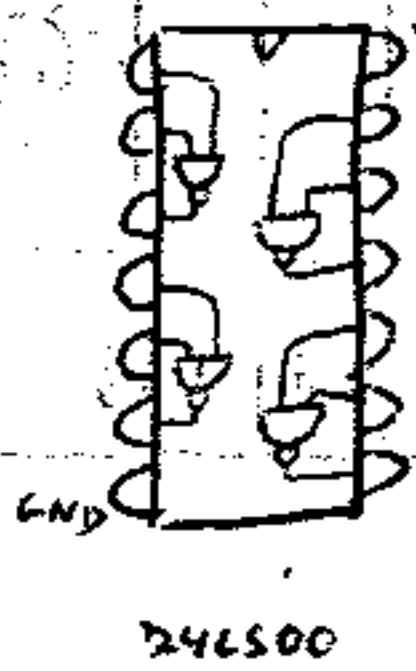
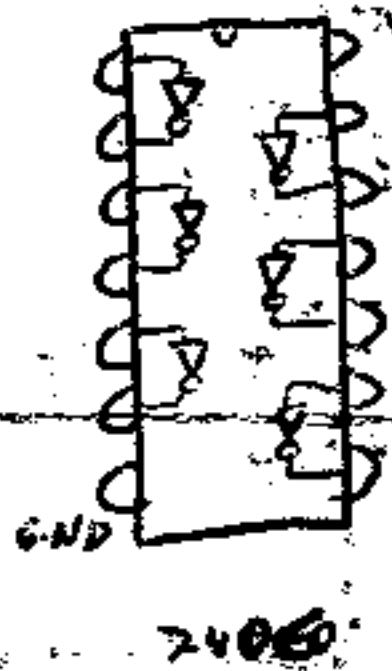
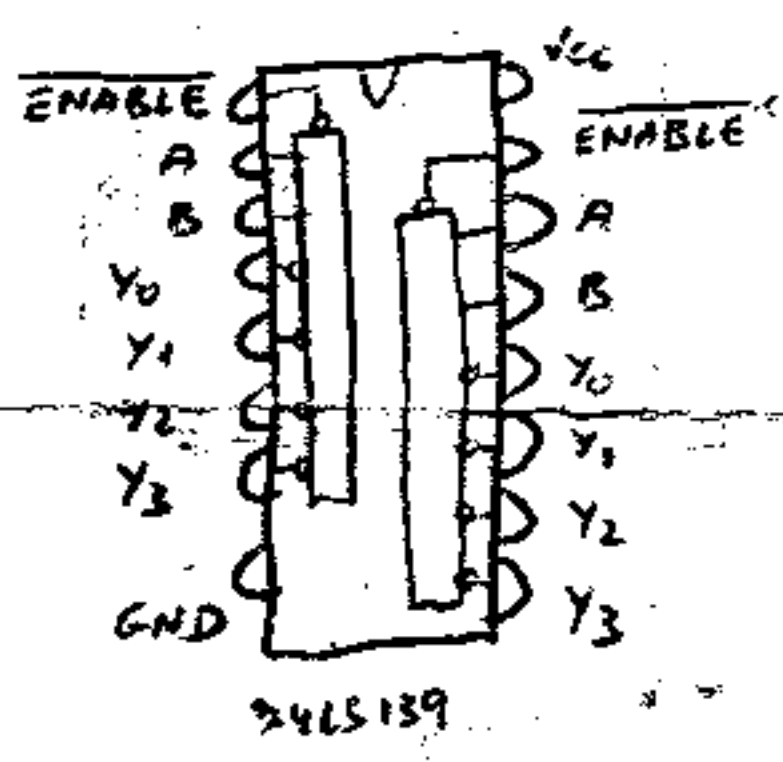
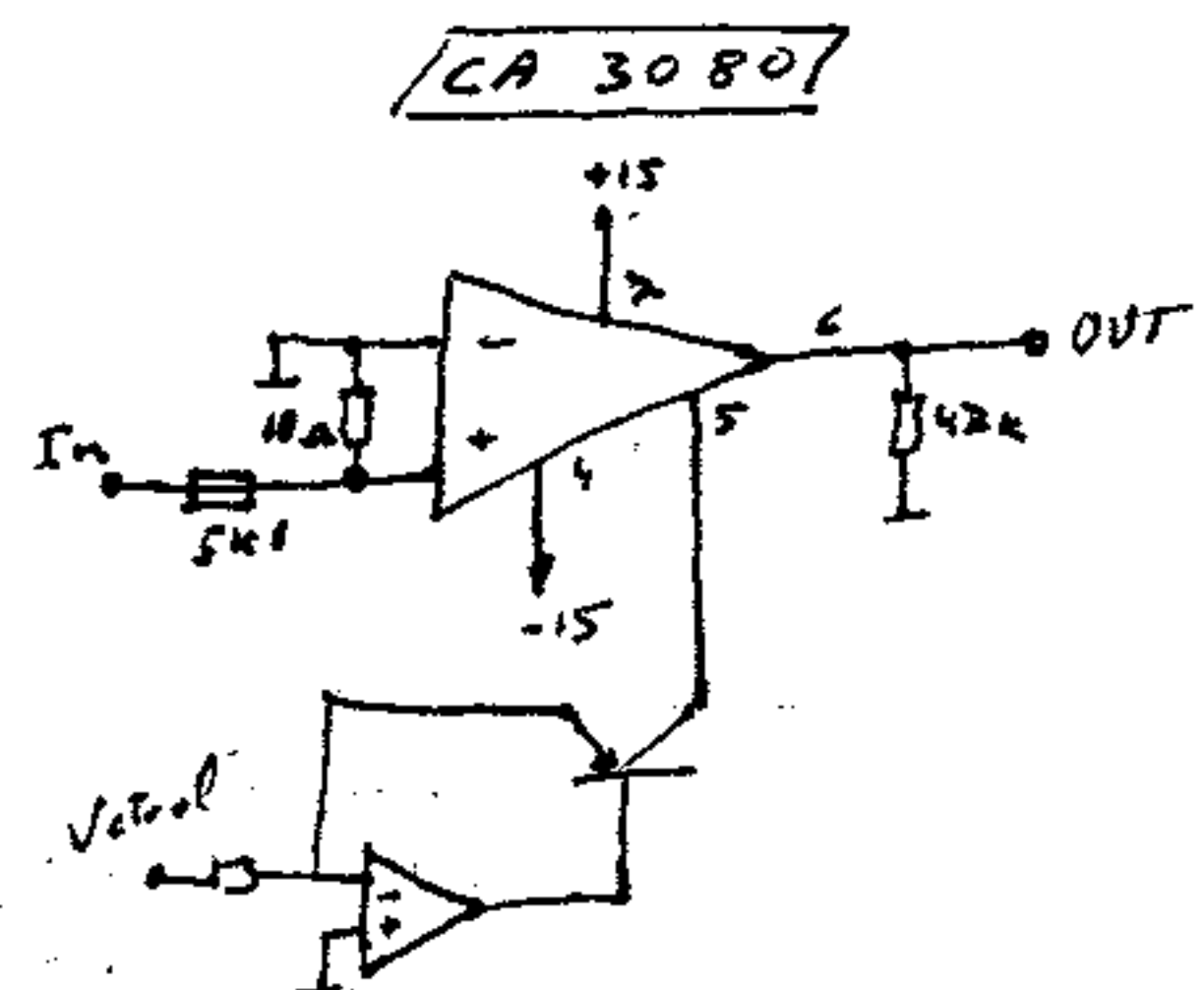
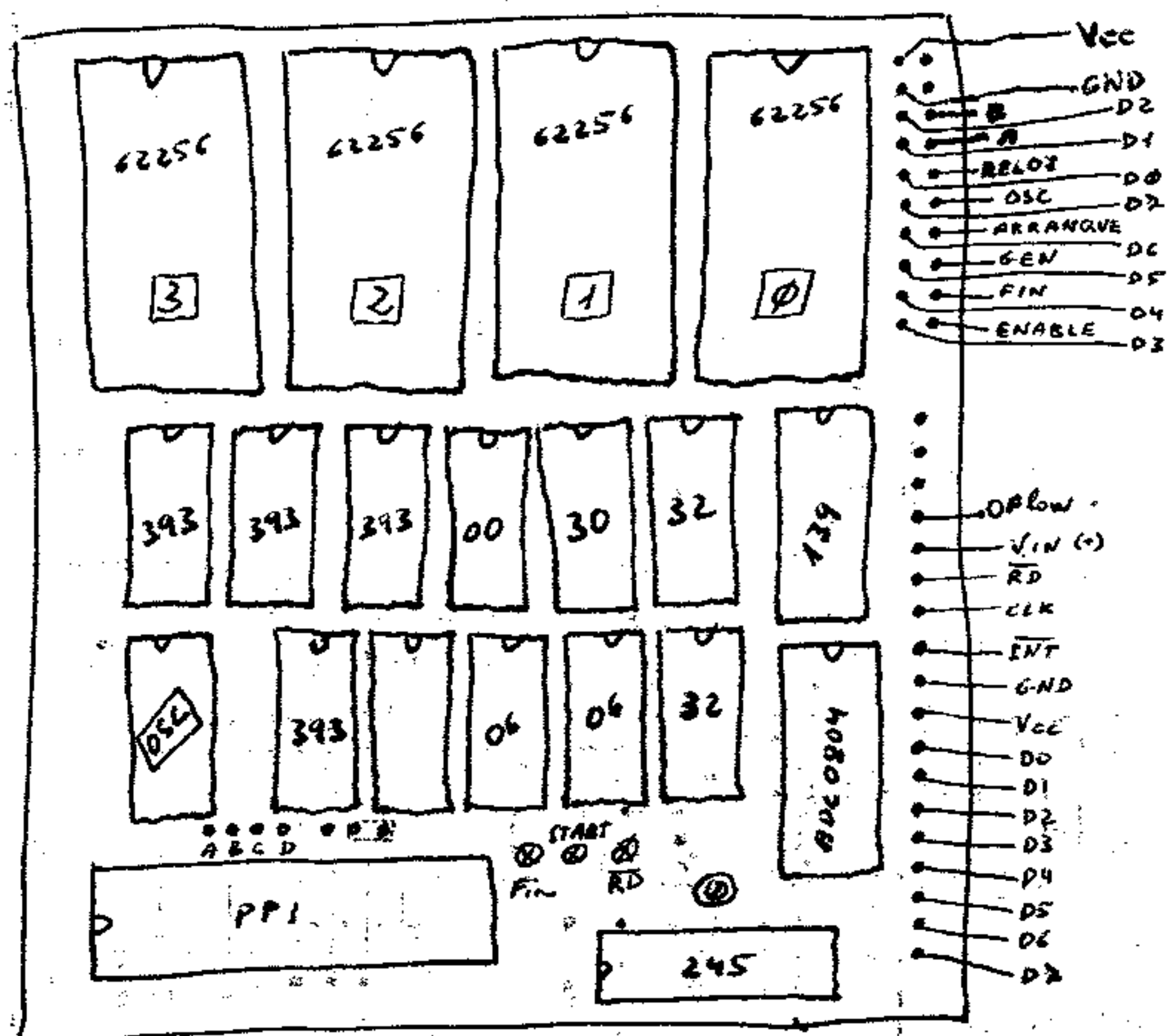
10/94

(A) = TIMER
 (B) = SCAN



Port	Use
E4	ETimer 300Hz
E5	301 (01) (01)
E6	302 (02) (02)
E7	IT (CW)
E8	303 (03)
E9	304 (04)
EA	305 (05)
EB	IT (CW)
EC	106 (06)
ED	107 (07)
EE	108 (08)
EF	IT (CW)
FD	Data
FI	Control
F2	Control (Fin)
F3	PPI (CW)





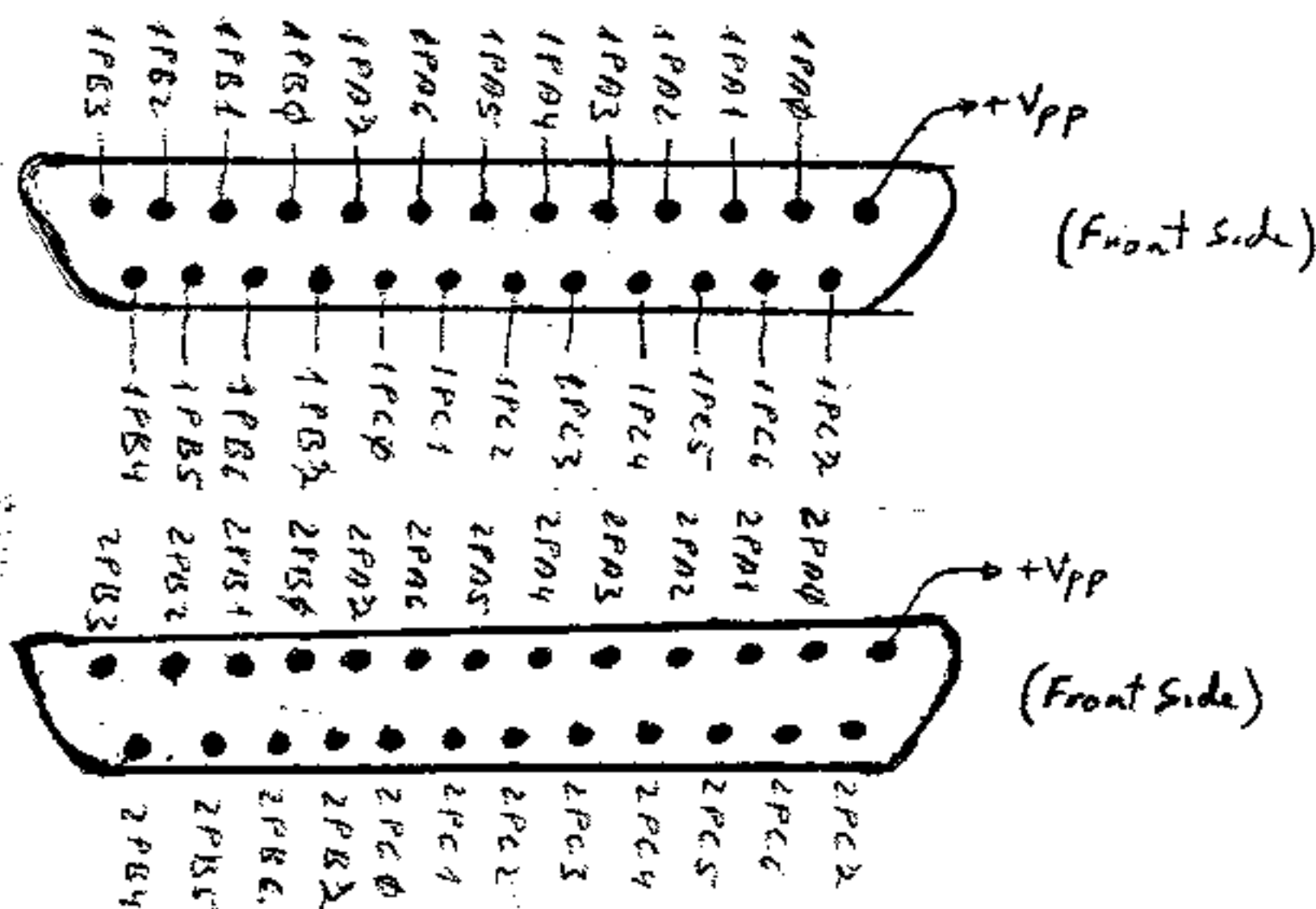
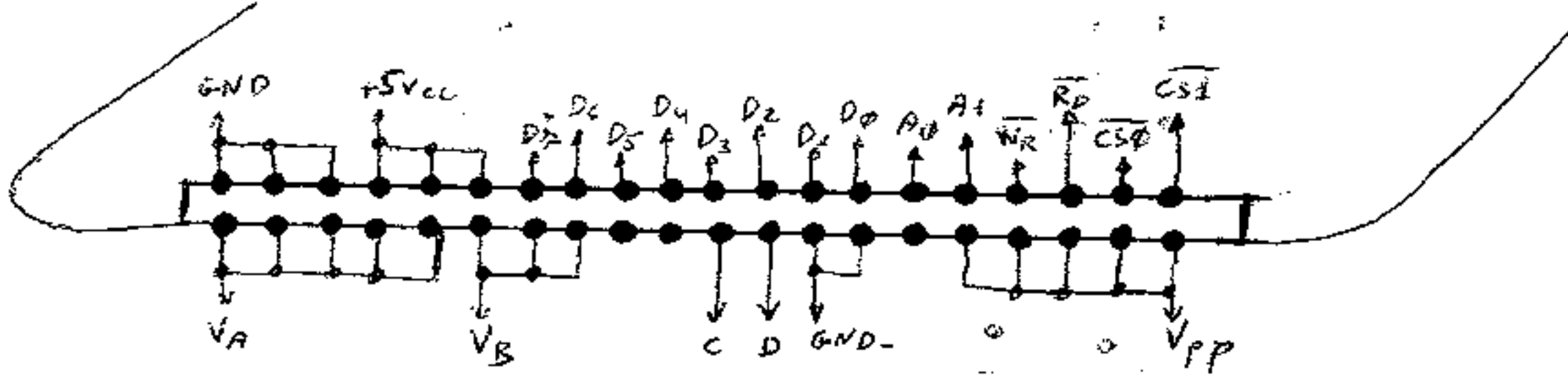
8255

24LS245

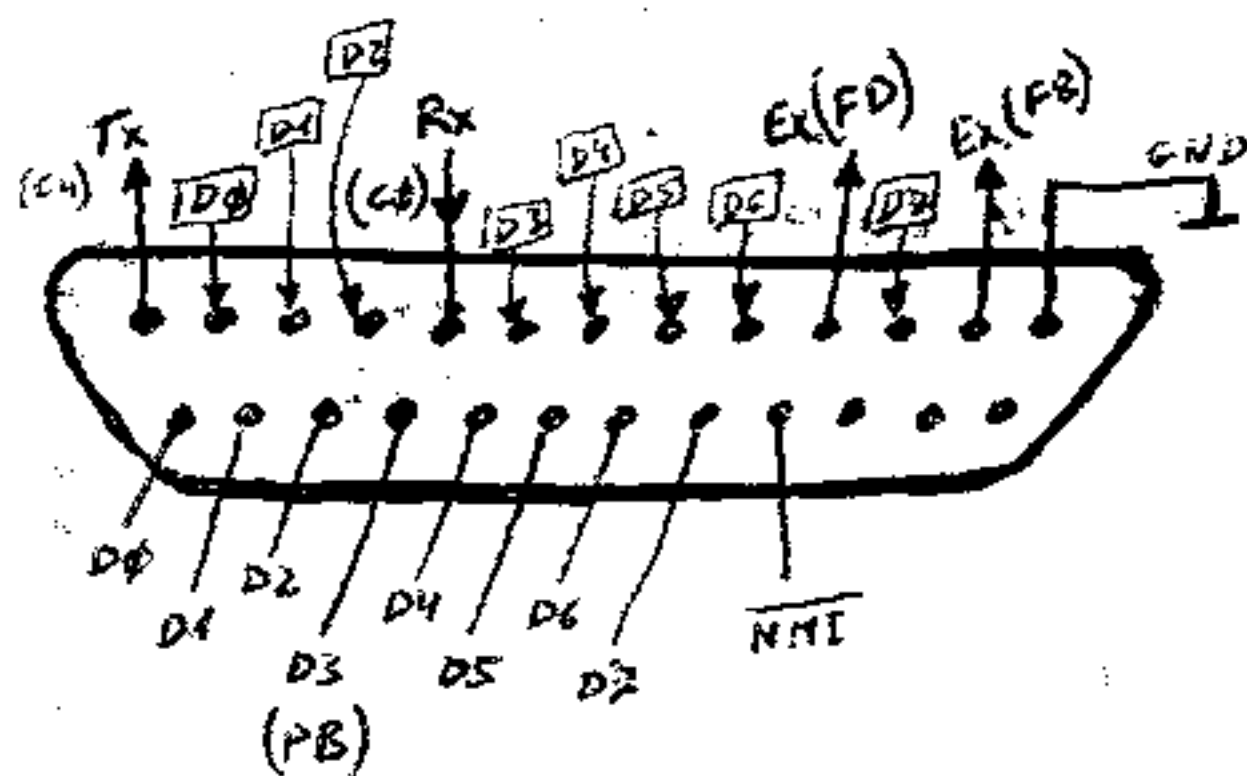
PORTS Map

@	HEX			
000	00	PW 5A 2.5-30V _{cc} (00-7F) Pw. Supply A		OUT
001	01	Rx-Tx DATA		IN/OUT
002	02	Rx-Tx FLAGS // Switches // Leds		IN/OUT
003	03	C.W.		IN
004	04	DISPLAY Segment		OUT
005	05	DISPLAY Digit		OUT
006	06	Key board & Display		IN/OUT
007	07	C.W.		IN
008	08	A PW		OUT
009	09	B DRIVERS 1		OUT
010	0A	C		OUT
011	0B	C.W.		IN
012	0C	A PW		OUT
013	0D	B DRIVERS 2		OUT
014	0E	C		OUT
015	0F	C.W.		IN
016	10	A LOGIC		IN/OUT
017	11	B IN - OUT 1		IN/OUT
018	12	C		IN/OUT
019	13	C.W.		IN
020	14	A LOGIC		IN/OUT
021	15	B IN - OUT 2		IN/OUT
022	16	C		IN/OUT
023	17	C.W.		IN
024	18	A LOGIC		IN/OUT
025	19	B IN - OUT 3		IN/OUT
026	1A	C		IN/OUT
027	1B	C.W.		IN
028	1C	PW 2A 2.5-30V _{cc} (80-FF) Pw Supply 2		OUT
029	1D	PW 2A 2.5-30V _{cc} (80-FF) Pw Supply 1		OUT
030	1E	A/D Channel Socket (8) (01001000) 2-Emul		OUT
031	1F	C.W.		IN

248	F8	NC	240	F0	Data (Internal)	E8	201	E0	
249	F9	NC	241	F1	CTrol	E9	202	E1	
250	FA	NC	242	F2	FIN	EA	203	E2	COMP
251	FB	NC	243	F3	CW PPI	EB	IT _{CW}	E3	OUT
252	FC	A/D Converter	244	F4		EC	101	E4	300
253	FD	A/D Converter	245	F5		ED	102	E5	301
254	FE	A/D Converter	246	F6	COMP. OUT	EE	103	E6	302
255	FF	A/D Converter	247	F7		EF	IT _{CW}	E7	IT _{CW}



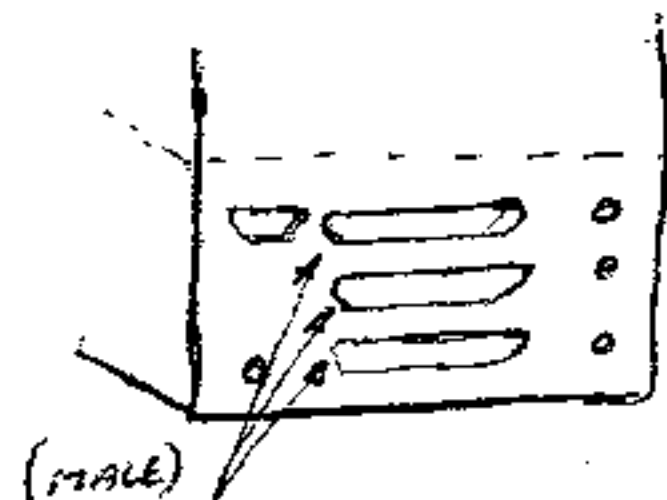
DRIVERS



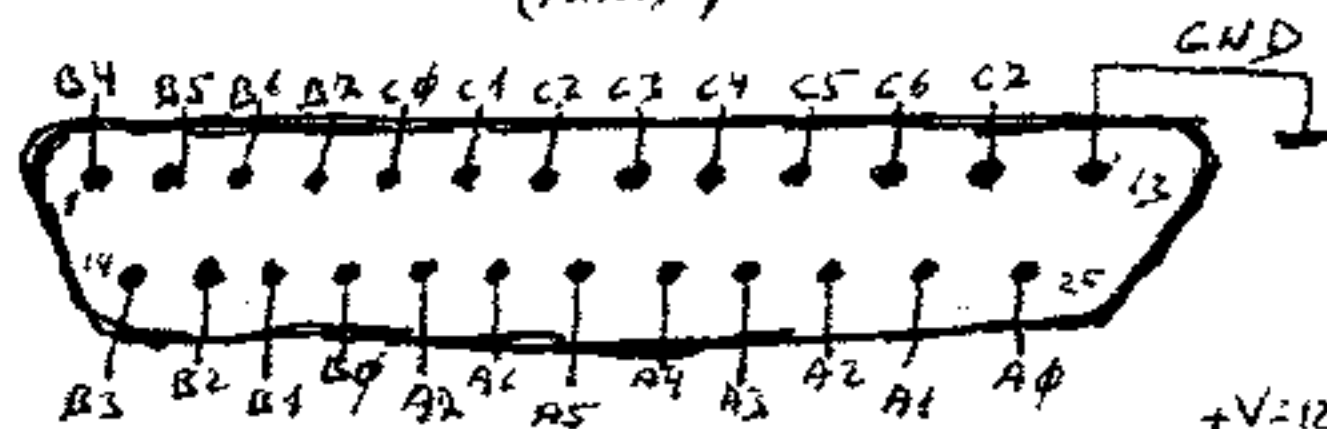
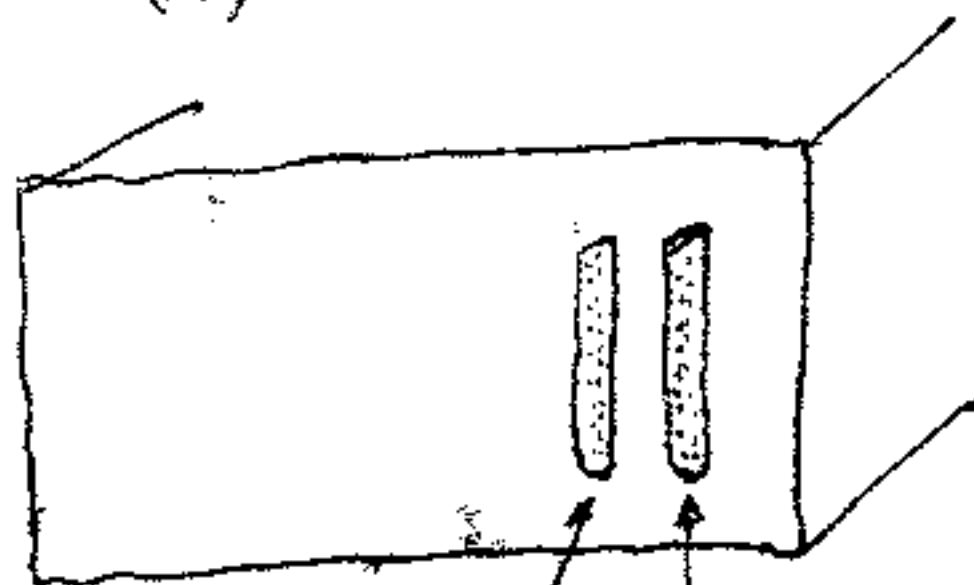
D0 - D7 ↔ PC (Port 882)
D0 - D2 ↔ SPECTRUM

COMUNICACIONES

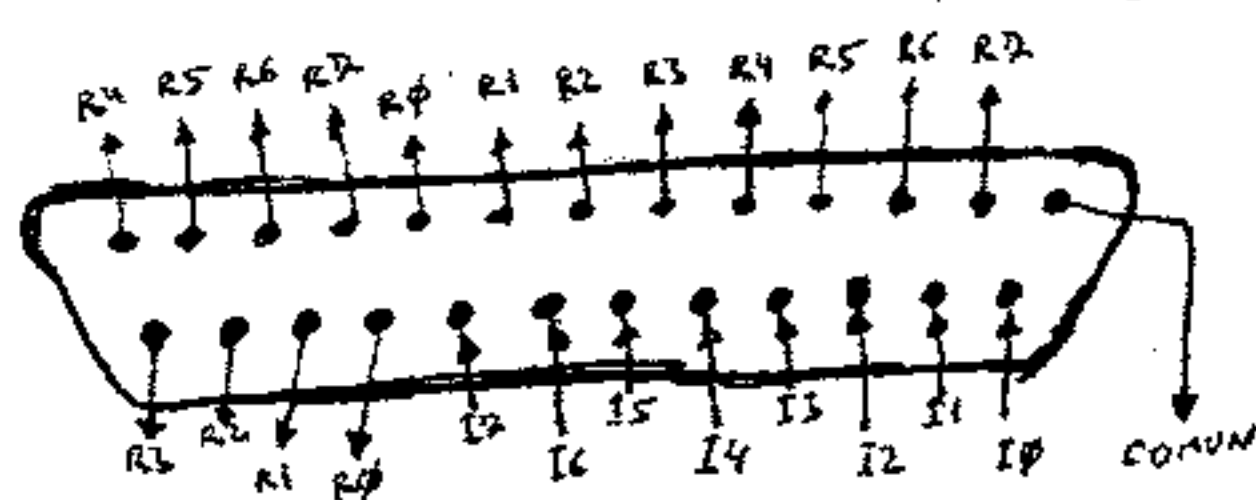
(Front Side)



(MALE)

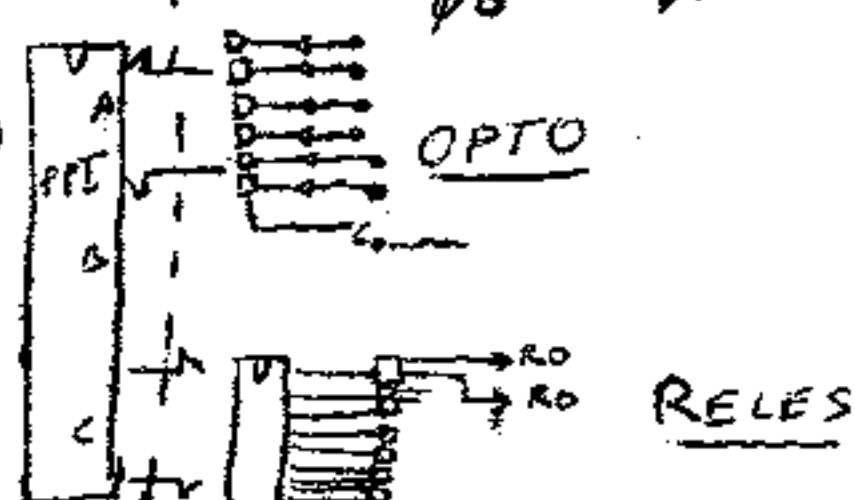


PPI



RELE & OPTO BOARD

RELE & OPTO



ROM MAP			RAM MAP			RAM MAP			
000	0000	INITIAL RESET	32268	8000	DELAY "CTE"	L	32800	8020	ANALOG VAR PORT
022	0048	VIN ROUTINE	69	01		H	32801	8021	N Var.
1112	045D	LEVEL 0	32270	8002	DELAY "HL"	L	32802	8022	PP Var
1346	0542	CTRL KEYS	21	03		H	03	23	
1624	0658	MAIN PGM	32222	8004			32804	8024	Pgm Add in Execution
1564	061C	CHECK IN ROUTINE (C.M)	23	05			05	25	(PC)
			24	06			32806	8026	Process "VAR"
			25	02			02	22	
			26	08			32808	8028	Delay "CTE"
			22	09			09	29	
			28	0A			32810	802A	CALL &
			29	0B			11	2B	RETURN
			80	0C			12	2C	ROUTINE
							13	2D	
2000		READ BLOCK 22C512	32281	800D	KEY CODE PULSED				
2031		WRITE BLOCK "	32282	800E	VALUE DATA Enter		32814	802E	VIN time on Change
206F		Verify CLEAR "	32283	800F	VALUE Add. Enter	L	15	2F	
20A4		Read ROM Add "	84	10		H	32816	8030	V1 IN (VIN) CHECK IN ROUTINE
20BD		Read Block 22C25C	32285	8011	KEY CODE Convert		32812	8031	V2 Ent (VIN) CHECK IN ROUTINE
20F2		WRITE BLOCK "	32286	8012	ROUTINE 2-4 Key : 2-0		32818	8032	MOTOR * (VAR)
2131		Read Add ROM "	32287	8013	Add Message Display	L	19	33	
2148		COPY ROUTINE	88	14		H	32820	8034	MOTOR * (VAR)
215A		CLEAR RAM Buffer	32289	8015	RESULT 255 = Si 0 = No		21	35	
			32290	8016	Rx - Tx leng	L	32822	8036	MOTOR * VAR
			91	12		H	23	32	
			32292	8018	Rx - Tx Add	L	32824	8038	VAR (d) 1
			93	14		H	32825	8039	VAR (d) 2
			32294	801A	Next Add	L			
			95	1B	(Rx - Tx) Pgm IN	H	33024	8100	TABLA
			32296	801C	Next Add	L			(DIONISOS)
			92	1D	(Rx - Tx) buff OUT	H	33229	81FF	
			32298	801E	SWITCHES				
			32299	801F	Analog Input		65535	FFFF	STACK ↑

DISPLAY MAP

13 7 15 5 4 3 2 1 13

DIONISOS

TABLA
(DIONISOS)