

Effect of Parasitic Capacitance in Op Amp Circuits

Application Report

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Contents

1	Introduction	1
2	Basic One-Pole Op Amp Model	2
3	Basic Circuits and Analysis	2
3.1	Gain Analysis	3
3.1.1	Stability Analysis	4
4	Capacitance at the Inverting Input	6
4.1	Gain Analysis with C_n	6
4.1.1	Stability Analysis with C_n	9
4.1.2	Compensating for the Effects of C_n	10
5	Capacitance at the Noninverting Input	13
5.1	Gain Analysis with C_p	13
5.2	Stability Analysis with C_p	14
5.3	Compensating for the Effects of C_p	14
6	Output Resistance and Capacitance	16
6.1	Gain Analysis with R_o and C_o	16
6.2	Stability Analysis with R_o and C_o	17
6.3	Compensation for R_o and C_o	18
7	Summary	24
8	References	25

List of Figures

1 Basic Dominant Pole Op Amp Model	2
2 Amplifier Circuits Constructed with Negative Feedback	2
3 Gain-Block Diagrams	3
4 Spice Simulation of Noninverting and Inverting Amplifier	4
5 Loop Gain Magnitude and Phase Plot	5
6 Adding Cn to Amplifier Circuits	6
7 Spice Simulation of Cn in Noninverting and Inverting Amplifiers	8
8 Loop Gain Magnitude and Phase Asymptote Plots with Cn	9
9 Simulation Results with C1 and C2 Added to Compensate for Cn	12
10 Effect of Cn in Inverting and Noninverting Amplifier	12
11 Adding Cp to Amplifier Circuits	13
12 Spice Simulation with Cp in Noninverting and Inverting Amplifier Circuits	14
13 Spice Simulation with Cs Added to Compensate for Cp in Noninverting Amplifier	15
14 Ro and Co Added to Amplifiers	16
15 Gain Block Diagrams with Ro and Co	16
16 Spice Simulation with Ro and Co	17
17 Loop Gain Magnitude and Phase with Ro and Co	18
18 Isolation Resistor Added to Isolate the Feedback Loop from Effects of Ro	19
19 Phase Shift in $\frac{V_{fb}}{aV_e}$ vs the Ratio Ri:Ro	20
20 Maximum Phase Shift in $\frac{V_{fb}}{aV_e}$ vs the Ratio Ri:Ro	20
21 Spice Simulation Results with Ri Added to Compensate for Ro and Co	21
22 Video Buffer Application	21
23 Ri and Cc Added to Compensate for Effects of Ro and Co	22
24 Simplified Feedback Models	22
25 Simulation of Feedback Using Ri and Cc to Compensate for Ro and Co	23

List of Tables

1 Noninverting Amplifier: Capacitor Location, Effect, and Compensation Summary	24
2 Inverting Amplifier: Capacitor Location, Effect, and Compensation Summary	24

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ABSTRACT

Parasitic capacitors are formed during normal op amp circuit construction. Op amp design guidelines usually specify connecting a small 20-pF to 100-pF capacitor between the output and negative input, and isolating capacitive loads with a small, 20-Ω to 100-Ω resistor. This application report analyzes the effects of capacitance at the input and output pins of an op amp, and suggests means for computing appropriate values for specific applications. The inverting and noninverting amplifier configurations are used for demonstration purposes. Other circuit topologies can be analyzed in a similar manner.

1 Introduction

Two conductors, insulated from one another, carrying a charge, and having a voltage potential between them, form a capacitor. Capacitors are characterized by their charge-to-voltage ratio; $C = \frac{q}{V}$, where C is the capacitance in Farads, q is the charge in Coulombs, and V is the voltage in volts. In general, capacitance is a function of conductor area, distance between the conductors, and physical properties of the insulator. In the special case of two parallel plates separated by an insulator $C = \frac{\epsilon\epsilon_0 \times A}{d}$ where ϵ is the dielectric constant of the insulator, ϵ_0 is the permittivity of free space, A is the area of the plates, and d is the distance between the plates. Thus, in general:

- Capacitance is directly proportional to the dielectric constant of the insulating material and area of the conductors.
- Capacitance is inversely proportional to the distance separating the conductors.

Rarely are two parallel plates used to make a capacitor, but in the normal construction of electrical circuits, an unimaginable number of capacitors are formed. On circuit boards, capacitance is formed by parallel trace runs, or traces over a ground or power plane. In cables there is capacitance between wires, and from the wires to the shield.

- Circuit traces on a PCB with a ground and power plane will be about 1–3 pF/in.
- Low capacitance cables are about 20–30 pF/ft conductor to shield.

Therefore, with a few inches of circuit board trace and the terminal capacitance of the op amp, it is conceivable that there can be 15–20 pF on each op amp terminal. Also, cables as short as a few feet can present a significant capacitance to the op amp.

This report assumes that a voltage feedback op amp is being used.

2 Basic One-Pole Op Amp Model

The voltage feedback op amp is often designed using dominant pole compensation. This gives the op amp a one-pole transfer function over the normal frequencies of operation that can be approximated by the model shown in Figure 1 (a). This model is used throughout this report in the spice simulations with the following values: $gm=0.1$, $R_c=1\text{ M}\Omega$ and $C_c=159\text{ nF}$. With these values, the model has the following characteristics: dc gain = 100 dB, dominant pole frequency = 10 Hz, and unity gain bandwidth = 1 MHz.

In the schematic drawings, the representation shown in Figure 1 (b) is used,

where
$$a = gm \times \frac{R_c}{1 + sR_cC_c}$$

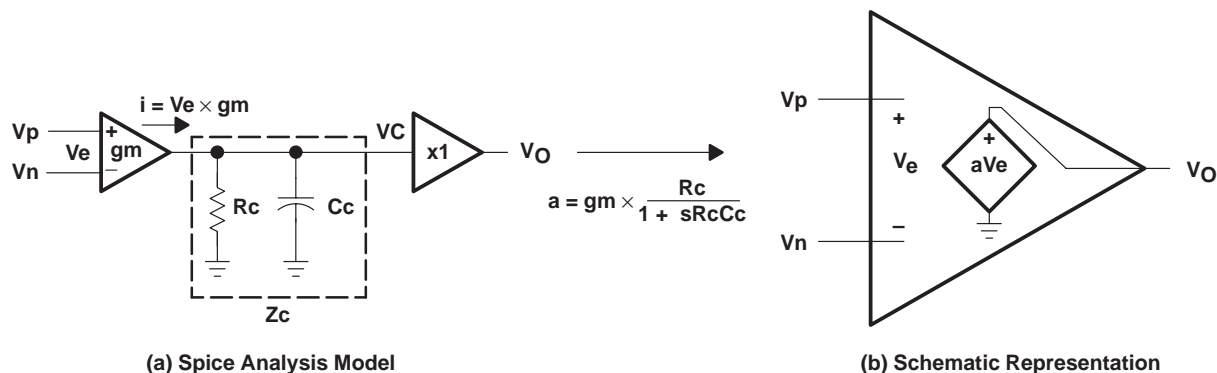


Figure 1. Basic Dominant Pole Op Amp Model

3 Basic Circuits and Analysis

Figure 2 (a) shows a noninverting amplifier and Figure 2 (b) shows an inverting amplifier. Both amplifier circuits are constructed by adding negative feedback to the basic op amp model.

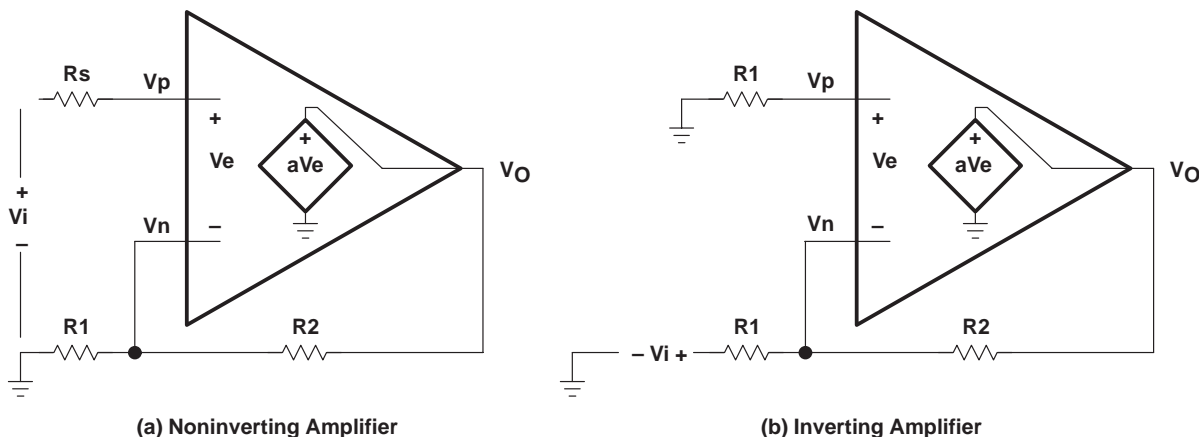


Figure 2. Amplifier Circuits Constructed with Negative Feedback

These circuits are represented in gain block diagram form as shown in Figure 3 (a) and (b). Gain block diagrams are a powerful tool in understanding gain and stability analysis.

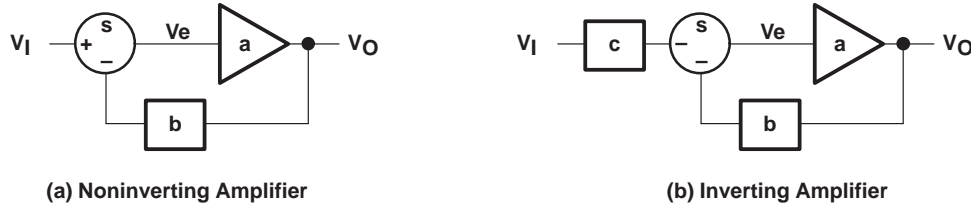


Figure 3. Gain-Block Diagrams

In the gain block diagrams:

$a = gm \times \frac{R_c}{1 + sR_cC_c}$, $b = \frac{R1}{R1 + R2}$, and $c = \frac{R2}{R1 + R2}$. Summing node s either inverts or passes unchanged each input—depending on the sign at the input—and adds the results together to produce the output.

3.1 Gain Analysis

In the gain block diagram of Figure 3 (a) (noninverting amplifier), $V_o = aV_e = a(V_i - bV_o)$. Solving the transfer function:

$$\frac{V_o}{V_i} = \left(\frac{1}{b}\right) \left[\frac{1}{1 + \frac{1}{ab}} \right] = \left(\frac{R1 + R2}{R1}\right) \left[\frac{1}{1 + \left(\frac{1 + sR_cC_c}{gmR_c}\right) \left(\frac{R1 + R2}{R1}\right)} \right] \quad (1)$$

This equation describes a single pole transfer function where $\frac{1}{b}$ is the dc gain and the pole is at the frequency where $\frac{1}{ab} = 1$

In the gain block diagram of Figure 3 (b) (inverting amplifier), $V_o = aV_e = a(-cV_i - bV_o)$. Solving the transfer function:

$$\frac{V_o}{V_i} = -\left(\frac{c}{b}\right) \left[\frac{1}{1 + \frac{1}{ab}} \right] = \left(\frac{R2}{R1}\right) \left[\frac{1}{1 + \left(\frac{1 + sR_cC_c}{gmR_c}\right) \left(\frac{R1 + R2}{R1}\right)} \right] \quad (2)$$

This equation describes a single pole transfer function where $-\frac{c}{b}$ is the dc gain and the pole is at the frequency where $\frac{1}{ab} = 1$.

Figure 4 shows the results of a spice simulation of the circuits with $R1$ and $R2 = 100 \text{ k}\Omega$, and $R_s = 50 \text{ k}\Omega$. As expected, the circuit gains are flat from dc to the point where $\frac{1}{ab} = 1$, and then roll-off at -20dB/dec . The open loop gain is plotted for reference.

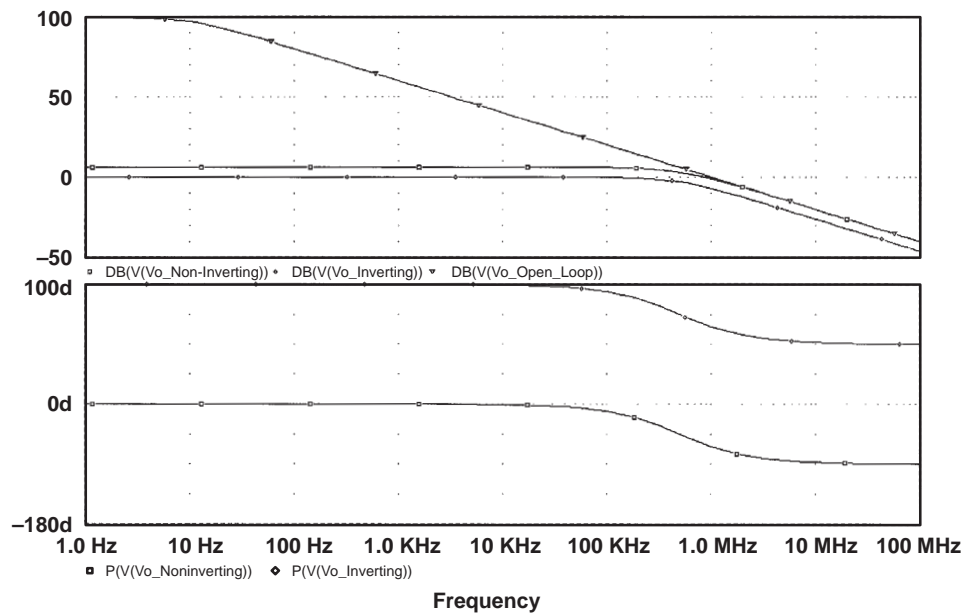


Figure 4. Spice Simulation of Noninverting and Inverting Amplifier

3.1.1 Stability Analysis

Using either gain block diagram, consider a signal traversing the loop from V_e , through the gain block a , to V_o , back through the gain block b , and the summing node s to V_e . If, while traversing this loop, the signal experiences a phase shift of 0° , or any integer multiple of 360° , and a gain equal to or greater than 1, it will reinforce itself causing the circuit to oscillate. Since there is a phase shift of 180° in the summing node s , this equates to:

$$|ab| \geq 1 \text{ \& } \angle ab = -180^\circ \rightarrow \text{Oscillation.}$$

In reality, anything close to this usually causes unacceptable overshoot and ringing.

The product of the open loop gain of the op amp, a , and the feedback factor, b , is of special significance and is often termed the loop gain or the loop transmission. To determine the stability of an op amp circuit, consider the magnitude, $|ab|$, and phase, $\angle ab$.

Figure 5 shows $\text{dB } |a|$ and $\text{dB } \frac{1}{b}$ plotted along with $\angle ab$ for the one-pole op amp model in either amplifier circuit with purely resistive feedback ($R_1=R_2=100\text{K}$). It is obvious that, since the maximum phase shift in $\angle ab$ is -90° , the circuits are stable.

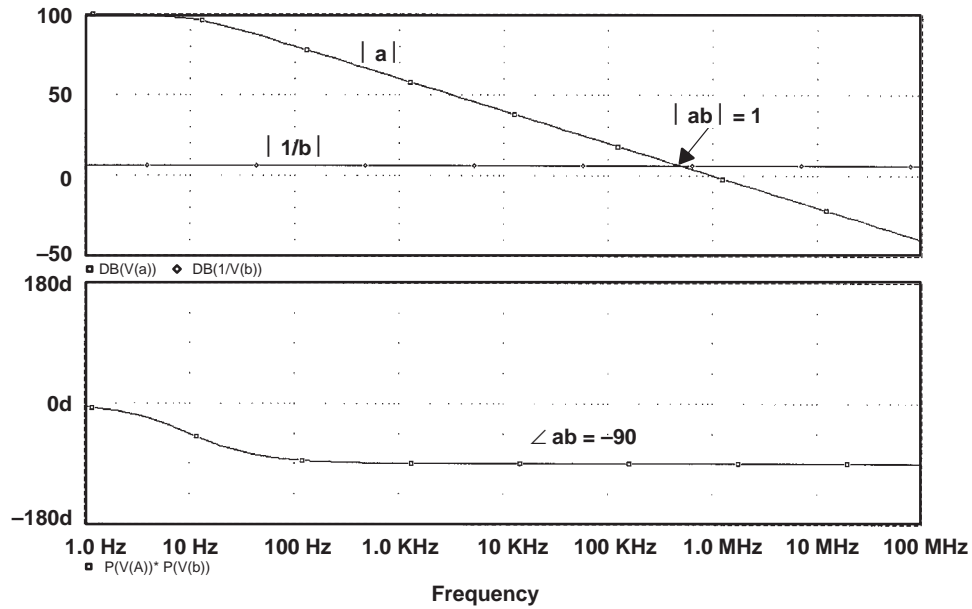


Figure 5. Loop Gain Magnitude and Phase Plot

At the point where $\text{dB } |a|$ and $\text{dB } \left| \frac{1}{b} \right|$ intersect, $\text{dB } |a| - \text{dB } \left| \frac{1}{b} \right| = 0$. This is the same as $\log |a| + \log |b| = 0$, and taking the anti-log; $|ab| = 1$.

The slope of $\text{dB } |a|$ or $\text{dB } \left| \frac{1}{b} \right|$ indicates their phase: $-40 \text{ dB/dec} = -180^\circ$, $-20 \text{ dB/dec} = -90^\circ$, $0 \text{ dB/dec} = 0^\circ$, $20 \text{ dB/dec} = 90^\circ$, $40 \text{ dB/dec} = 180^\circ$, etc. Since $\left| \frac{1}{b} \right|$ is the inverse of $|b|$, the sign of its phase is opposite, i.e., if $\angle b = -90^\circ$ then $\angle \frac{1}{b} = 90^\circ$. Therefore a rate of closure $= 40 \text{ dB/dec}$ between $\text{dB } |a|$ and $\text{dB } \left| \frac{1}{b} \right|$ indicates $\angle ab = -180^\circ$ and the circuit is normally unstable. Plotting $\text{dB } |a|$ and $\text{dB } \left| \frac{1}{b} \right|$ on a log scale gives a visual indication of the stability of the circuit.

4 Capacitance at the Inverting Input

Figure 6 (a) and (b) show adding C_n to the noninverting and inverting amplifier circuits.

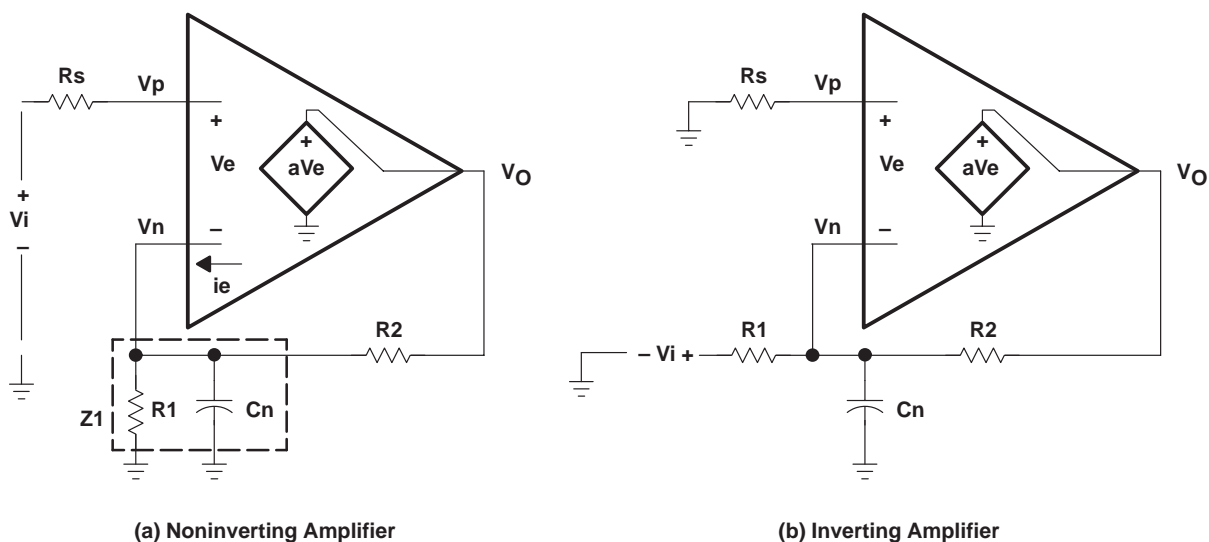


Figure 6. Adding C_n to Amplifier Circuits

4.1 Gain Analysis with C_n

Making use of the block diagrams and their related circuit solutions, determine how C_n has modified the gain block values and substitute as required.

For the noninverting amplifier shown in Figure 6 (a):

$$V_n = V_o \frac{Z_1}{Z_1 + R_2}$$

where $Z_1 = \frac{R_1}{1 + sR_1C_n}$.

Solving for the modified feedback factor:

$$b = \frac{Z_1}{Z_1 + R_2} = \left(\frac{R_1}{1 + sR_1C_n} \right) \left(\frac{1}{\left(\frac{R_1}{1 + sR_1C_n} \right) + R_2} \right) = \frac{1}{\frac{R_1 + R_2}{R_1} + sR_2C_n} \quad (3)$$

For the inverting amplifier shown in Figure 6 (b) writing the node equation at V_n results in:

$$\frac{V_n - V_i}{R_1} + V_n sC_n + \frac{V_n - V_o}{R_2} = 0.$$

Therefore,

$$\begin{aligned}
 V_n &= V_i \left(\frac{R_2}{R_1 + R_2 + sC_n R_1 R_2} \right) + \left(\frac{V_o(R_1)}{R_1 + R_2 + sC_n R_1 R_2} \right) \\
 &= V_i \left[\frac{1}{\frac{R_1 + R_2}{R_2} + sC_n R_1} \right] + V_o \left[\frac{1}{\frac{R_1 + R_2}{R_1} + sC_n R_2} \right]
 \end{aligned}$$

As above:

$$b = \frac{1}{\frac{R_1 + R_2}{R_1} + sR_2 C_n}, \text{ and } c = \frac{1}{\frac{R_1 + R_2}{R_2} + sR_1 C_n}$$

Using these values in the solutions to the gain block diagrams of Figure 3, the noninverting amplifier's gain, with C_n added to the circuit, is:

$$\frac{V_o}{V_i} = \left(\frac{1}{b} \right) \left[\frac{1}{1 + \frac{1}{ab}} \right] = \left(\frac{R_1 + R_2}{R_1} + sR_2 C_n \right) \left[\frac{1}{1 + \left(\frac{1 + sR_c C_c}{gmR_c} \right) \left(\frac{R_1 + R_2}{R_1} \right)} \right] \quad (4)$$

and the inverting amplifier's gain, with C_n added to the circuit, is:

$$\begin{aligned}
 \frac{V_o}{V_i} &= - \left(\frac{c}{b} \right) \left[\frac{1}{1 + \frac{1}{ab}} \right] = - \left[\frac{\frac{R_1 + R_2}{R_1} + sR_2 C_n}{\frac{R_1 + R_2}{R_2} + sR_1 C_n} \right] \left[\frac{1}{1 + \left(\frac{1 + sR_c C_c}{gmR_c} \right) \left(\frac{R_1 + R_2}{R_1} + sR_2 C_n \right)} \right] \\
 &= - \left(\frac{R_2}{R_1} \right) \left[\frac{\frac{R_1 + R_2}{R_2} + sR_1 C_n}{\frac{R_1 + R_2}{R_2} + sR_1 C_n} \right] \left[\frac{1}{1 + \left(\frac{1}{a} \right) \left(\frac{R_1 + R_2}{R_1} + sR_2 C_n \right)} \right] \\
 &= - \left(\frac{R_2}{R_1} \right) \left[\frac{1}{1 + \left(\frac{1 + sR_c C_c}{gmR_c} \right) \left(\frac{R_1 + R_2}{R_1} + sR_2 C_n \right)} \right]
 \end{aligned} \quad (5)$$

Figure 7 shows the results of a spice simulation of both amplifiers with $C_n = 15.9 \text{ nF}$, resistors R_1 and $R_2 = 100 \text{ k}\Omega$, and $R_s = 50 \text{ k}\Omega$. Refer to it while taking a closer look at Equations 4 and 5.

In Equation 4, the first term

$$\left(\frac{R_1 + R_2}{R_1} + sR_2 C_n \right)$$

contains a zero at

$$f_z = \frac{R_1 + R_2}{2\pi R_1 R_2 C_n}.$$

In the spice simulation we see effects of this zero as the gain begins to increase at around 200 Hz. In the second term of Equation 4, substitute

$R_m = \frac{1}{gm}$, to get

$$\left(\frac{1}{1 + \left(\frac{R_m}{R_c} + sR_mC_c \right) \left(\frac{R_1 + R_2}{R_1} + sR_2C_n \right)} \right)$$

$$= \frac{1}{s^2(R_mC_cR_2C_n) + s \left(R_2C_n \frac{R_m}{R_c} + R_mC_c \frac{R_1 + R_2}{R_1} \right) + 1 + \left(\frac{R_m}{R_c} \right) \left(\frac{R_1 + R_2}{R_1} \right)}$$

Solving the characteristic equation for s^2 in the denominator we find that the transfer function has a complex conjugate pole at $s_{1,2} = -660 \pm j62890$. Taking only the dominant terms in the equation, the double pole can be approximated in the frequency domain at:

$$P_{1,2} = \frac{1}{2\pi \sqrt{R_mC_cR_2C_n}} = 10 \text{ kHz},$$

with the model values as simulated. At this frequency the denominator tends to zero and the gain theoretically increases toward infinity. What we see on the simulation results is peaking in the gain plot and a rapid 180° phase shift in the phase plot at 10 kHz. The circuit is unstable.

In Equation 5, notice that the frequency effects of the capacitor cancel out of the first term of the transfer function. The simulation results show the gain is flat until the second term, which is identical to Equation 4, causes peaking in the gain plot, and a rapid 180° phase shift in the phase plot at 10 kHz. This circuit is also unstable.

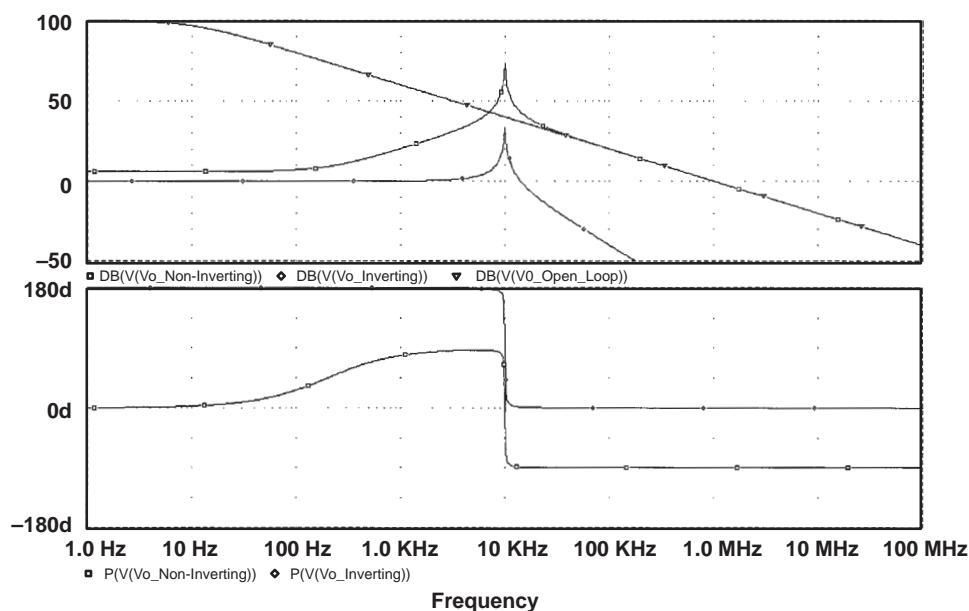


Figure 7. Spice Simulation of C_n in Noninverting and Inverting Amplifiers

4.1.1 Stability Analysis with C_n

To analyze stability with C_n added to the amplifier circuit, use the modified feedback factor,

$$b = \frac{1}{\frac{R1+R2}{R1} + sR2Cn}$$

At low frequencies where

$$\frac{R1+R2}{R1} \gg 2\pi fR2Cn, \frac{1}{b} \cong \frac{R1+R2}{R1}$$

and the plot is flat ($\angle b = 0^\circ$). As frequency increases, eventually $\frac{R1+R2}{R1} = 2\pi fR2Cn$. At this frequency $\left|\frac{1}{b}\right| = \left(\frac{R1+R2}{R1}\right)(\sqrt{2})$ ($\angle b = -45^\circ$). Above this frequency $\left|\frac{1}{b}\right|$ increases at 20dB/dec ($\angle b = -90^\circ$). Depending on the value of C_n , there are two possible scenarios:

1. The break frequency is below the frequency where $\left|\frac{1}{b}\right|$ and $|a|$ intersect. This causes the rate of closure between $\left|\frac{1}{b}\right|$ and $|a|$ to be 40dB/dec. This is an unstable situation and will cause oscillations (or peaking) near this frequency. Reference $\frac{1}{b1}$ in Figure 8 and the results of the spice simulation shown in Figure 7.
2. The break frequency is above the frequency where $\left|\frac{1}{b}\right|$ and $|a|$ intersect. There is no effect in the pass band of the amplifier. Reference $\frac{1}{b2}$ in Figure 8.

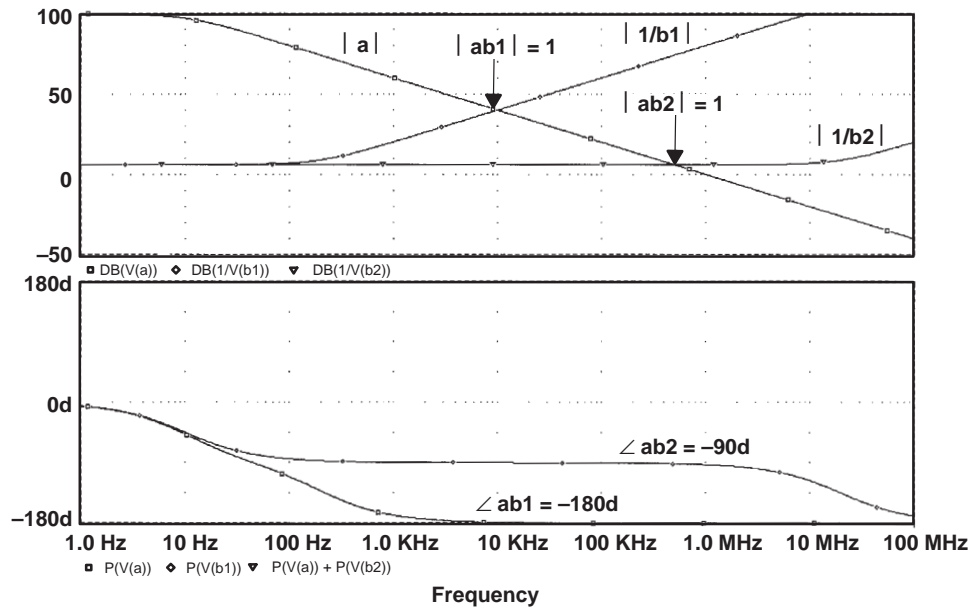


Figure 8. Loop Gain Magnitude and Phase Asymptote Plots with C_n

4.1.2 Compensating for the Effects of C_n

1. Reduce the value of C_n by removing ground or power plane around the circuit trace to the inverting input.
2. Reduce the value of R_2 .
3. For noninverting amplifier, place a capacitor $C_2 = C_n \frac{R_1}{R_2}$ in parallel with R_2 .
4. For inverting amplifier, place a capacitor $C_2 = C_n \frac{R_1}{R_2}$ in parallel with R_2 , and place a capacitor $C_1 = C_n$ in parallel with R_1 .

Methods 1 and 2 attempt to move the effect of C_n to a higher frequency where it does not interfere with normal operation.

Method 3 is used for the noninverting amplifier. It cancels the effect of C_n .

To solve the modified transfer function with C_2 in parallel with R_2 , substitute Z_2 for R_2 , where $Z_2 = \frac{R_2}{1 + sR_2C_2}$, in the derivation of b so that:

$$b = \frac{V_n}{V_o} = \frac{Z_1}{Z_1 + Z_2} = \left[\frac{\left(\frac{R_1}{1 + sR_1C_n} \right)}{\left(\frac{R_1}{1 + sR_1C_n} \right) + \left(\frac{R_2}{1 + sR_2C_2} \right)} \right] = \frac{1}{1 + \left(\frac{R_2}{R_1} \right) \left(\frac{1 + sR_1C_n}{1 + sR_2C_2} \right)} \quad (6)$$

By setting $C_2 = C_n \frac{R_1}{R_2}$, Equation 6 becomes:

$$b = \frac{1}{1 + \left(\frac{R_2}{R_1} \right) \left(\frac{1 + sR_1C_n}{1 + sR_1C_n} \right)} = \frac{1}{\left(\frac{R_1 + R_2}{R_1} \right)} = \left(\frac{R_1}{R_1 + R_2} \right).$$

Therefore, with the proper value of C_2 the effect of C_n is cancelled and the feedback factor looks purely resistive.

This works so well for the noninverting amplifier, let's investigate doing the same thing with the inverting amplifier. Placing $C_2 = C_n \frac{R_1}{R_2}$ across R_2 will cancel the effect of C_n so that b is purely resistive as shown above, but it causes another problem. Recalculating c with C_2 added we find:

$$c = \frac{Z_2}{R_1 + Z_2} \text{ where } Z_2 = \frac{R_2}{1 + sR_2C_2 || C_n} = \frac{1}{\frac{1}{R_2} + sC_x} \text{ where } C_x = C_2 || C_n.$$

In the transfer function, $\frac{V_o}{V_i} = -\left(\frac{c}{b}\right) \left[\frac{1}{1 + \frac{1}{ab}} \right]$, the second term is fine, but expanding out the first term we find:

$$\left(\frac{c}{b}\right) = \left(\frac{R2}{1 + sR2Cx}\right) \left[\frac{1}{R1 + \frac{R2}{1 + sR2Cx}} \right] \left(\frac{R1 + R2}{R1}\right) = \left(\frac{R2}{R1}\right) \left[\frac{1}{1 + \frac{sR1R2Cx}{R1 + R2}} \right]$$

Obviously we now have a pole in the transfer function at $f_p = 2\pi Cx \left(\frac{R1 + R2}{R1R2} \right)$ that limits the circuit's bandwidth. To cancel this pole, a zero needs to be added to the transfer function. Placing a capacitor, $C1$, across $R1$ will create a zero in the transfer function.

Again c and b need to be recalculated. We already have the solution in the form of Equation 6, and by proper substitution:

$$b = \frac{Vn}{Vo} = \left[\frac{\left(\frac{R1}{1 + sR1Cn||C1} \right)}{\left(\frac{R1}{1 + sR1Cn||C1} \right) + \left(\frac{R2}{1 + sR2C2} \right)} \right] = \frac{1}{1 + \left(\frac{R2}{R1} \right) \left(\frac{1 + sR1Cn||C1}{1 + sR2C2} \right)} \quad (7)$$

$$c = \frac{Vn}{Vi} = \left[\frac{\left(\frac{R2}{1 + sR2Cn||C2} \right)}{\left(\frac{R2}{1 + sR2Cn||C2} \right) + \left(\frac{R1}{1 + sR1C1} \right)} \right] = \frac{1}{1 + \left(\frac{R1}{R2} \right) \left(\frac{1 + sR2Cn||C2}{1 + sR1C1} \right)}$$

$$\left(\frac{c}{b}\right) = \frac{1 + \left(\frac{R2}{R1} \right) \left(\frac{1 + sR1Cn||C1}{1 + sR2C2} \right)}{1 + \left(\frac{R1}{R2} \right) \left(\frac{1 + sR2Cn||C2}{1 + sR1C1} \right)}$$

Setting $C2 = (Cn||C1) \frac{R1}{R2}$ in the numerator, simultaneously with setting $C1 = (Cn||C2) \frac{R2}{R1}$ in the denominator, results in cancellation. The problem is that this cannot be simultaneously achieved.

To arrive at a suitable compromise, assume that placing $C2 = Cn \frac{R1}{R2}$ across $R2$ cancels the effect of Cn in the feedback path as described above. Then, isolate the signal path between Vi and Vn by assuming $R2$ is open. With this scenario, Cn is acting with $R1$ to create a pole in the input signal path and placing an equal value capacitor in parallel with $R1$ will create a zero to cancel its effect.

Figure 9 shows the results of a spice simulation where methods 3 and 4 are used to compensate for $Cn = 15.9$ nF. $C2 = 15.9$ F in the noninverting amplifier and $C1 = C2 = 15.9$ F in the inverting amplifier. In both amplifier circuits, resistors $R1$ and $R2 = 100$ k Ω , and $Rs = 50$ k Ω . The plots show excellent results.

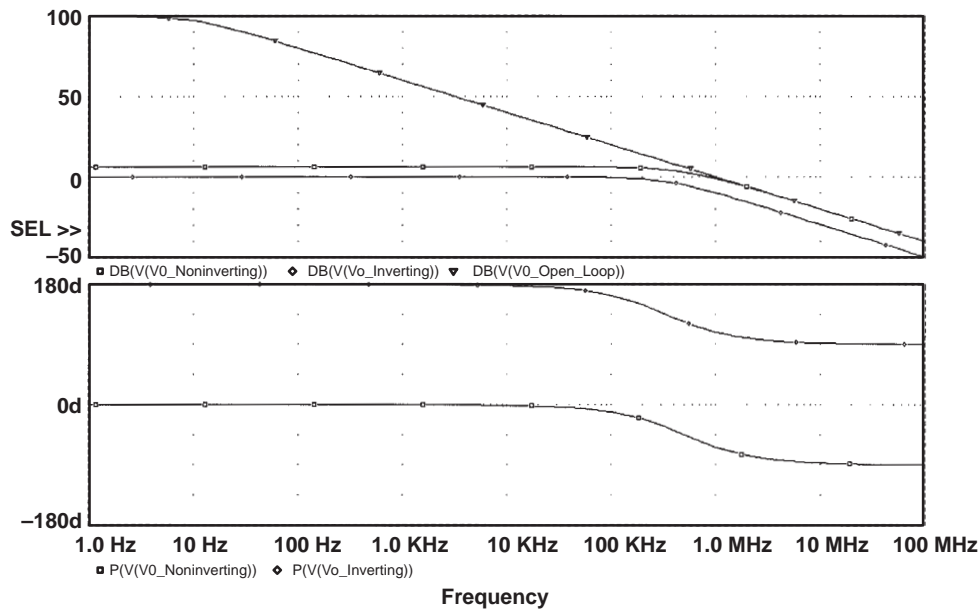


Figure 9. Simulation Results with C1 and C2 Added to Compensate for C_n

The action of any op amp operated with negative feedback is such that it tries to maintain 0 V across the input terminals. In the inverting amplifier, the op amp works to keep 0V (and thus 0 charge) across C_n . Because capacitance is the ratio of charge to potential, the effective capacitance of C_n is greatly reduced. In the noninverting amplifier C_n is charged and discharged in response to V_i . Thus the impact of C_n depends on topology. Lab results verify that, in inverting amplifier topologies, the effective value of C_n will be reduced by the action of the op amp, and tends to be less problematic than in noninverting topologies. Figure 10 shows that the effects of adding C_n to a noninverting amplifier are much worse than adding 10 times the same amount to an inverting amplifier with similar circuit components.

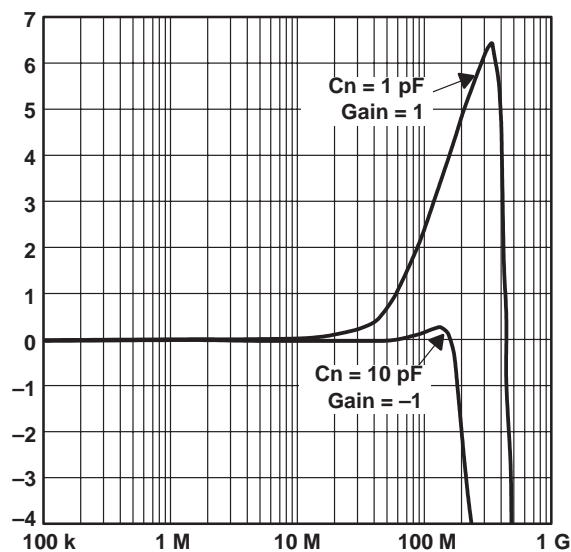


Figure 10. Effect of C_n in Inverting and Noninverting Amplifier

5 Capacitance at the Noninverting Input

In Figure 11 C_p is added to the amplifier circuits.

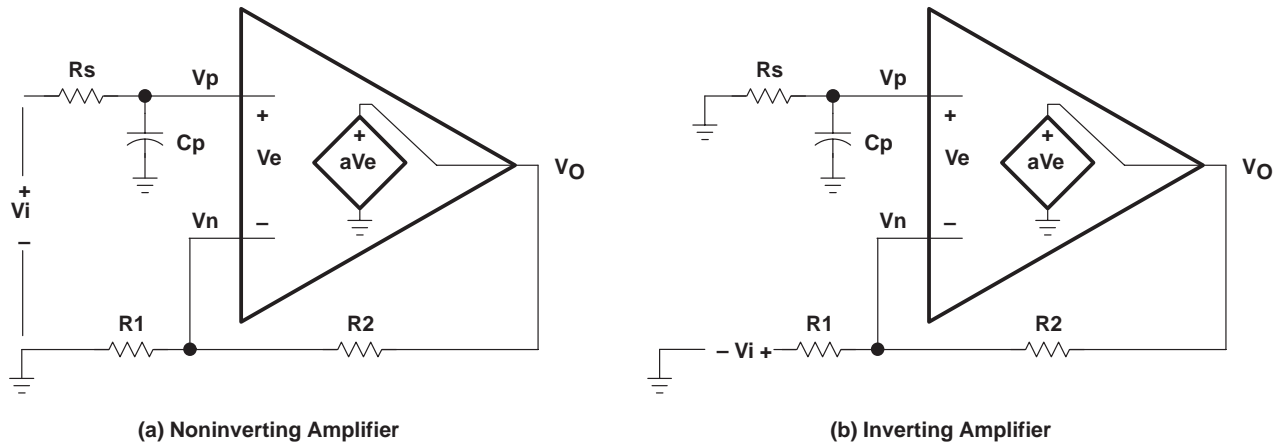


Figure 11. Adding C_p to Amplifier Circuits

5.1 Gain Analysis with C_p

In the case of the noninverting amplifier, the voltage seen at the noninverting input is modified so that $V_p = V_i \left(\frac{1}{1 + sR_sC_p} \right)$. Thus there is a pole in the input signal path before the signal reaches the input of the op amp. R_s and C_p form a low pass filter between V_i and V_p . If the break frequency is above the frequency at which $\left| \frac{1}{b} \right|$ intersects $|a|$, there is no effect on the operation of the circuit in the normal frequencies of operation.

The gain of the inverting amplifier is not affected by adding C_p to the circuit.

Figure 14 shows the results of a spice simulation where $C_p = 15.9$ nF. In both amplifier circuits, resistors R_1 and $R_2 = 100$ k Ω , and $R_s = 50$ k Ω . The plot shows a pole in the transfer function of the noninverting amplifier, whereas the inverting amplifier is unaffected.

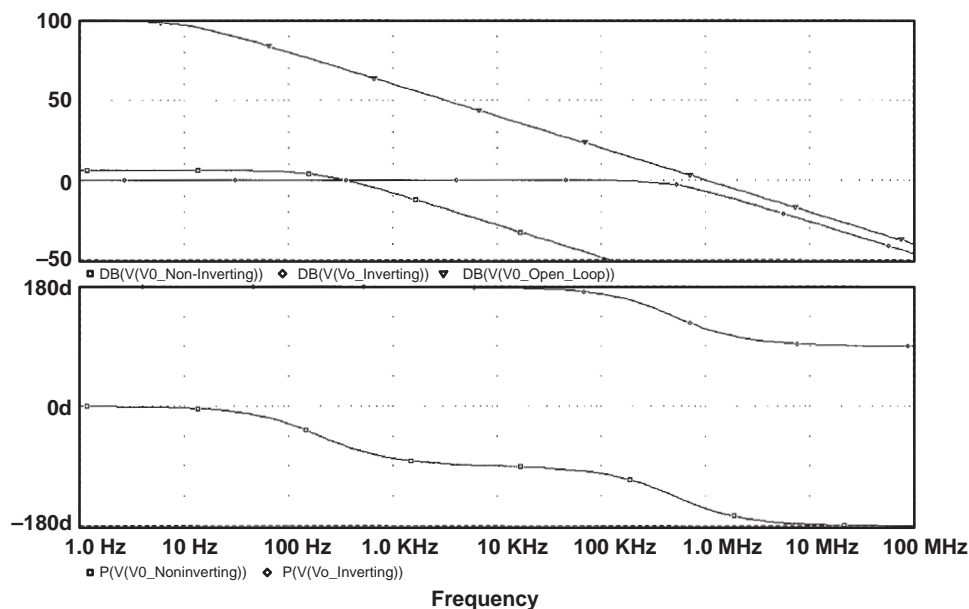


Figure 12. Spice Simulation with C_p in Noninverting and Inverting Amplifier Circuits

5.2 Stability Analysis with C_p

There is no change in the loop gain and thus no effect on stability for either amplifier circuit.

5.3 Compensating for the Effects of C_p

To compensate for the effect of capacitance at the noninverting input:

1. Reduce the value of C_p by removing ground or power plane around the circuit trace to the noninverting input.
2. Reduce the value of R_s .
3. Place a capacitor, C_s , in parallel with R_s so that $C_s \gg C_p$.

Methods 1 and 2 attempt to move the effect of C_p to a higher frequency where it does not affect transmission of signals in the pass band of the amplifier.

Method 3 tries to cancel the effect of C_p . The modified transfer function with C_s in parallel with R_s is:

$$\frac{V_p}{V_i} = \left(\frac{1 + sR_sC_s}{1 + sR_s(C_p + C_s)} \right) \quad (8)$$

$$\text{If } C_s \gg C_p, \text{ then } \left(\frac{1 + sR_sC_s}{1 + sR_s(C_p + C_s)} \right) \cong 1 \text{ and } V_p \cong V_i.$$

Figure 13 shows the results of a spice simulation of the previous noninverting amplifier circuit where a 159-nF and a 1.59- μ F capacitor is placed in parallel with R_s to compensate for $C_p = 15.9$ nF. The plot shows that a 10:1 ratio is good—loss of 1 db in gain at higher frequencies, but with a 100:1 ratio the effects of C_p are undetectable.

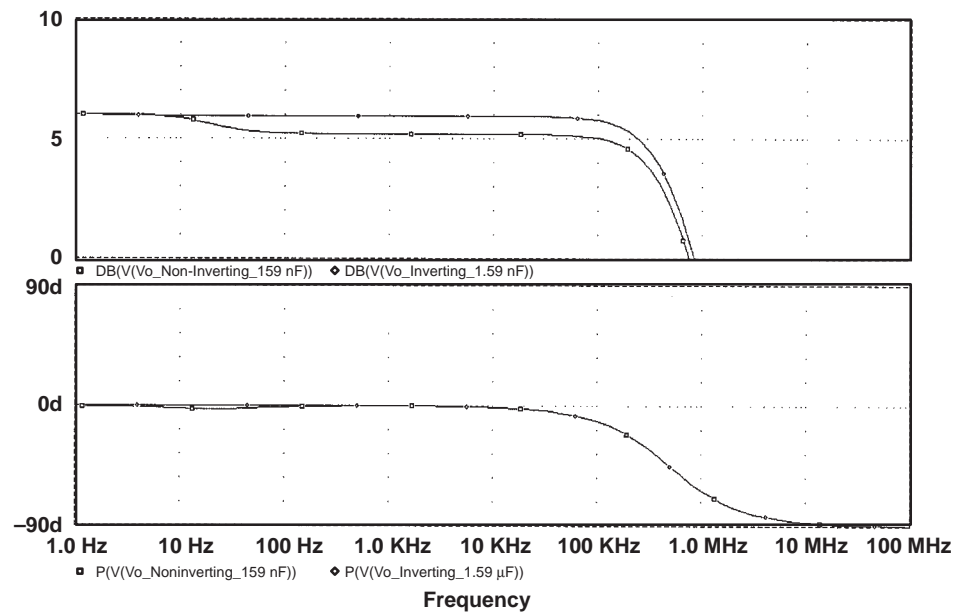


Figure 13. Spice Simulation with C_s Added to Compensate for C_p in Noninverting Amplifier

6 Output Resistance and Capacitance

Figure 14 shows R_o and C_o added to the amplifier circuits. R_o represent the output resistance of the op amp and C_o represents the capacitance of the load.

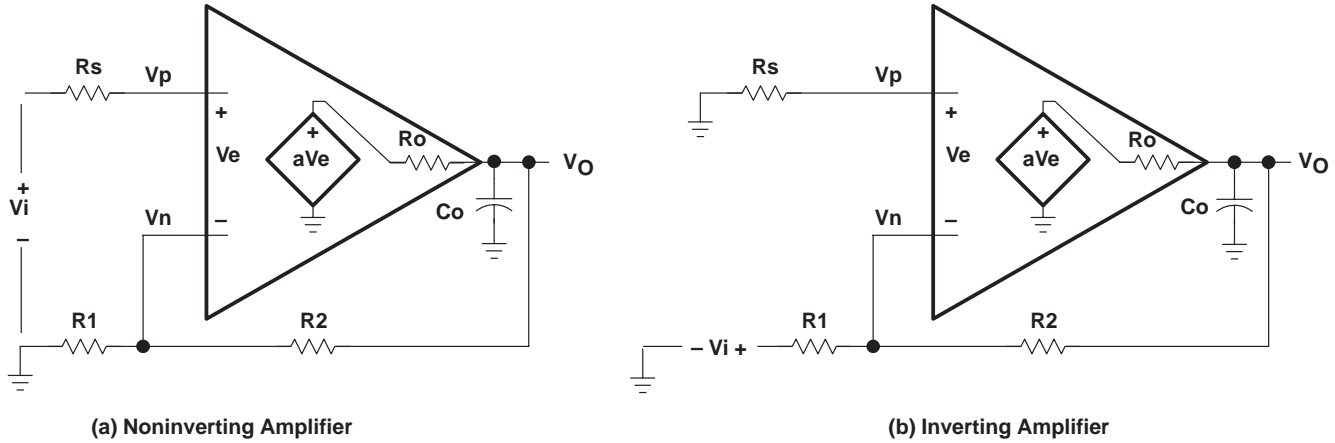


Figure 14. R_o and C_o Added to Amplifiers

6.1 Gain Analysis with R_o and C_o

Assuming that the impedance of R_2 is much higher than the impedance of R_o and C_o , the gain block diagrams for the amplifiers are modified to those shown in Figure 15 where:

$$d = \frac{V_o}{aVe} = \frac{1}{1 + sR_oC_o}$$

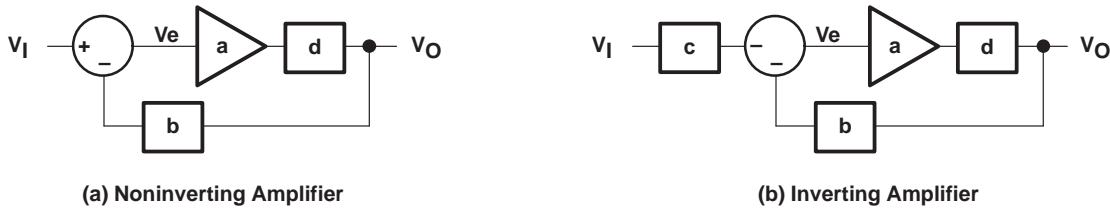


Figure 15. Gain Block Diagrams with R_o and C_o

Using Figure 15 (a), we calculate the transfer function of the noninverting amplifier:

$$\frac{V_o}{V_i} = \frac{1}{b} \left[\frac{1}{1 + \frac{1}{abd}} \right] = \left(\frac{R_1 + R_2}{R_1} \right) \left[\frac{1}{1 + \left(\frac{1 + sR_oC_o}{gmR_c} \right) \left(\frac{R_1 + R_2}{R_1} \right) (1 + sR_oC_o)} \right] \quad (9)$$

Using Figure 15 (b), we calculate the transfer function of the inverting amplifier:

$$\frac{V_o}{V_i} = -\left(\frac{c}{b} \right) \left[\frac{1}{1 + \frac{1}{abd}} \right] = -\left(\frac{R_2}{R_1} \right) \left[\frac{1}{1 + \left(\frac{1 + sR_oC_o}{gmR_c} \right) \left(\frac{R_1 + R_2}{R_1} \right) (1 + sR_oC_o)} \right] \quad (10)$$

Figure 16 shows the results of a spice simulation with $R_o = 100 \Omega$ and $C_o = 159 \mu\text{F}$. Resistors R_1 and $R_2 = 100 \text{ k}\Omega$, and $R_s = 50 \text{ k}\Omega$. Refer to the simulation results while taking a closer look at the second term of Equations 9 and 10. Expanding the denominator of second term with $R_m = \frac{1}{g_m}$ and collecting s terms:

$$s^2(R_m C_c R_o C_o) \left(\frac{R_1 + R_2}{R_1} \right) + s \left(R_o C_o \left(\frac{R_m}{R_c} \right) + R_m C_c \right) \left(\frac{R_1 + R_2}{R_1} \right) + 1 + \left(\frac{R_m}{R_c} \right) \left(\frac{R_1 + R_2}{R_1} \right)$$

Solving the characteristic equation for s^2 , the transfer function has a complex conjugate pole at $s_{1,2} = -63 + j14,063$. Taking only the dominant terms in the equation, the double pole can be approximated in the frequency domain at:

$$f_{p1,2} \cong \frac{1}{2\pi \sqrt{R_m C_c R_o C_o \left(\frac{R_1 + R_2}{R_1} \right)}} = 2.2 \text{ kHz},$$

with the model values as simulated. At this frequency the second term's denominator tends to zero and the gain theoretically increases to infinity. What we see on the simulation results at 2.2 kHz is significant peaking in the gain, and a rapid 180° phase shift. The circuit is unstable.

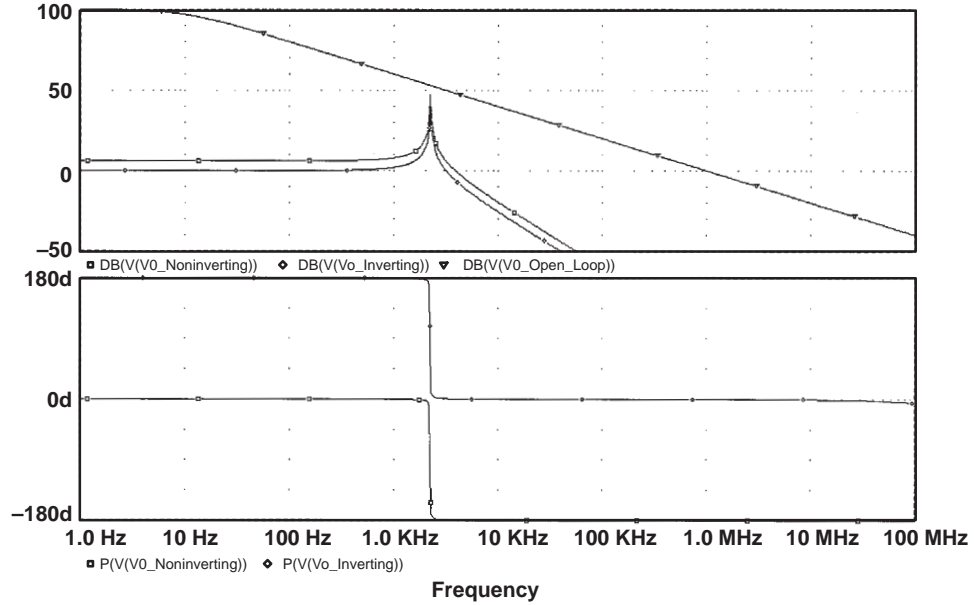


Figure 16. Spice Simulation with R_o and C_o

6.2 Stability Analysis with R_o and C_o

By the gain block diagrams shown in Figure 15 (a) and (b), the loop gain is now $= abd$ for both circuits. Since gain blocks a and b are not changed, to determine the stability of the circuit, the effect of gain block d is analyzed.

As noted above, $d = \frac{V_o}{aV_e} = \frac{1}{1 + sR_oC_o}$. At low frequencies where $1 \gg 2\pi fR_oC_o$, $\frac{1}{d} \cong 1$ and the plot is flat ($\angle d = 0^\circ$). As frequency increases, eventually $2\pi fR_oC_o = 1$. At this frequency $\left|\frac{1}{d}\right| = (\sqrt{2})$, and $\angle d = -45^\circ$. Above this frequency $\left|\frac{1}{d}\right|$ increases at 20dB/dec, and $\angle d = -90^\circ$. Depending on the value of R_o and C_o , there are two possible scenarios:

1. The break frequency is below the frequency where $\left|\frac{1}{bd}\right|$ and $|a|$ intersect. This causes the rate of closure to be 40dB/dec. This is an unstable situation and will cause oscillations (or peaking) near this frequency. Reference $\left|\frac{1}{bd1}\right|$ in Figure 17 and the results of the spice simulation shown in Figure 16.
2. The break frequency is above the frequency where $\left|\frac{1}{bd}\right|$ and $|a|$ intersect.

There is no effect in the pass band of the amplifier. Reference $\left|\frac{1}{bd2}\right|$ in Figure 17.

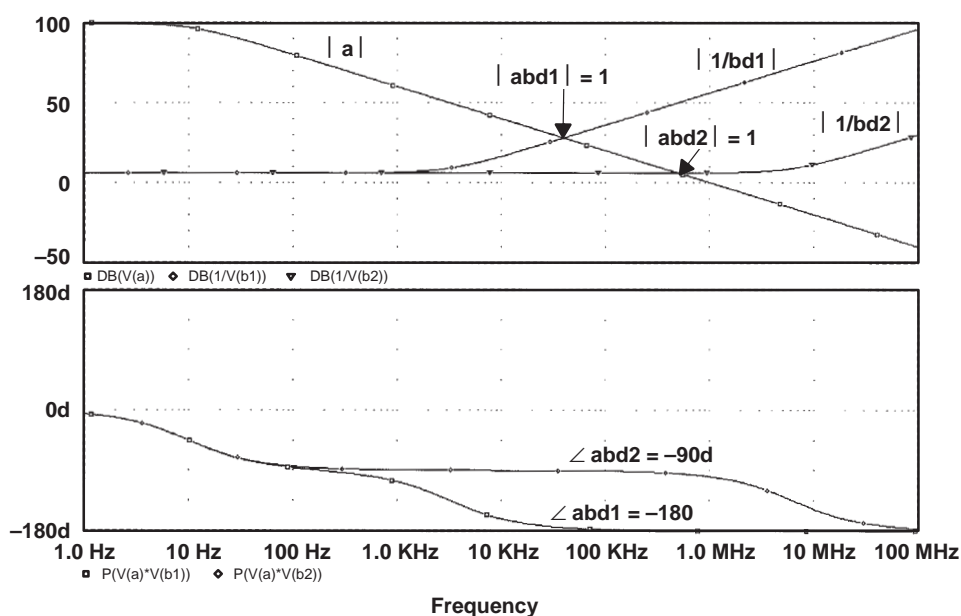


Figure 17. Loop Gain Magnitude and Phase with R_o and C_o

6.3 Compensation for R_o and C_o

To compensate for the effect of capacitance at the output:

1. Reduce the value of C_o by removing ground or power plane around the circuit trace to the output.
2. Reduce the value of C_o by minimizing the length of output cables.
3. Isolate the output pin from C_o with a series resistor.
4. Isolate the output pin from C_o with a series resistor, and provide phase lead compensation with a capacitor across R_2 .

Methods 1 and 2 seek to minimize the value of Co and thus its effects, but there is a limit to what can be done. In some cases, you will still be left with a capacitance that is too large for the amplifier to drive. Then method 3 or 4 can be used depending on your requirements.

Method 3 can be used if the resistive load is insignificant, or it is known and constant. Figure 18 shows the circuit modified with Ri added to isolate Co . By observation, adding Ri increases the phase shift seen at Vo , but now the feedback is taken from node Vfb .

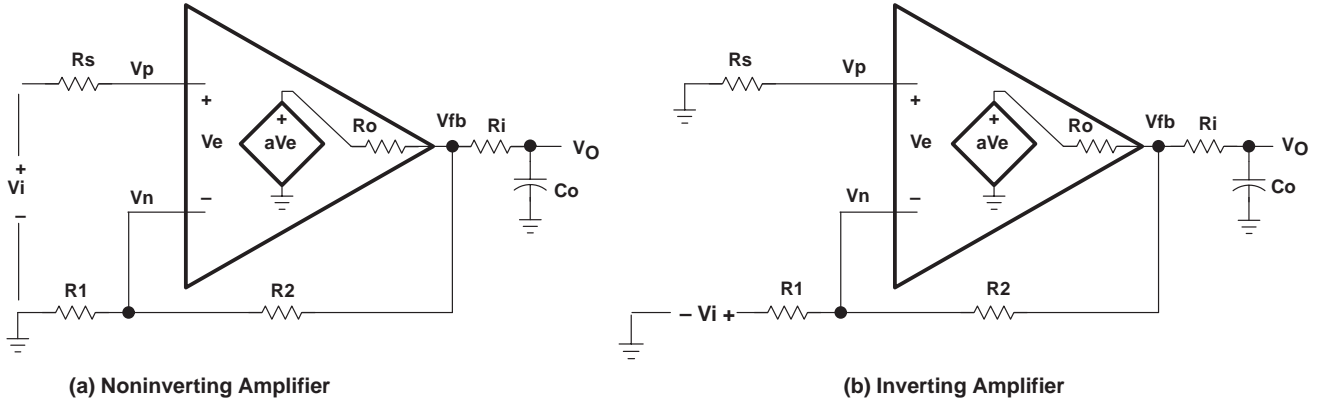


Figure 18. Isolation Resistor Added to Isolate the Feedback Loop from Effects of Ro

This modifies the gain block d . Making the assumption that the impedance of Ro , Ri , and Co is small compared to $R2$ then:

$$d = \frac{Vfb}{aVe} = \left[\frac{Ri + \frac{1}{sCo}}{Ro + Ri + \frac{1}{sCo}} \right] = \frac{1}{\frac{Ro}{Ri} + 1 + \frac{1}{sRiCo}} + \frac{1}{1 + sCo(Ri + Ro)}$$

Letting $z = \frac{1}{\frac{Ro}{Ri} + 1 + \frac{1}{sRiCo}}$ and $p = \frac{1}{1 + sCo(Ri + Ro)}$: $d = z + p$. z is a zero and p is a pole. Both have the same corner frequency; $f_{z,p} = \frac{1}{2\pi Co(Ri + Ro)}$. When $f < f_{z,p}$, or when $f > f_{z,p}$ the phase is zero. The ratio of $Ri:Ro$ determines the maximum phase shift near $f_{z,p}$.

Figure 19 shows a plot of the phase shift of $\frac{Vfb}{aVe}$ versus frequency with various ratios of $Ri:Ro$ and Figure 20 plots the maximum phase shift vs. the ratio of $Ri:Ro$. Depending on how much the phase margin can be eroded, a ratio can be chosen to suit. Note that the amount of phase shift depends only on the resistor ratio, not the resistor or capacitor values (these set the frequency $f_{z,p}$).

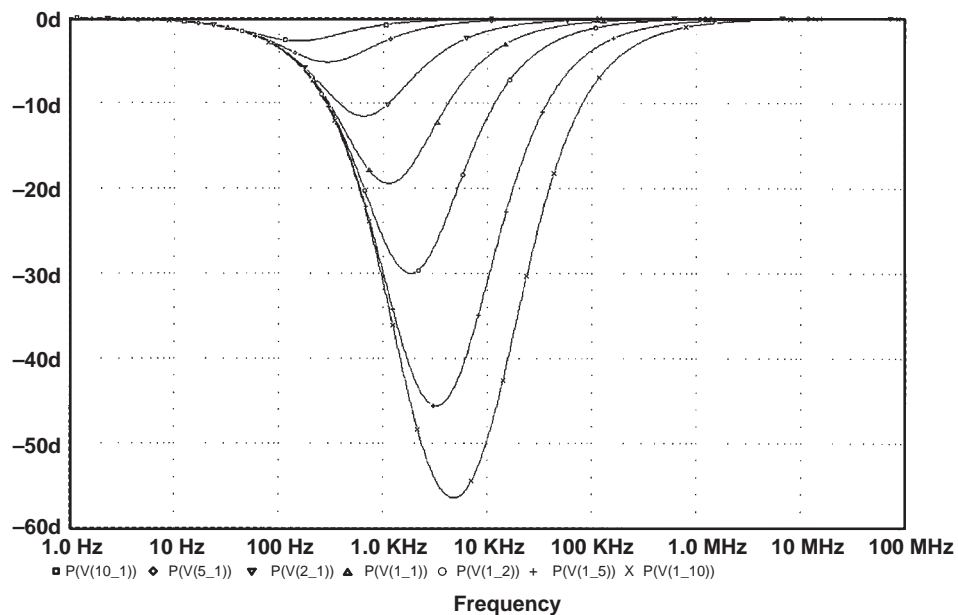


Figure 19. Phase Shift in $\frac{V_{fb}}{aV_e}$ vs the Ratio $R_i:R_o$

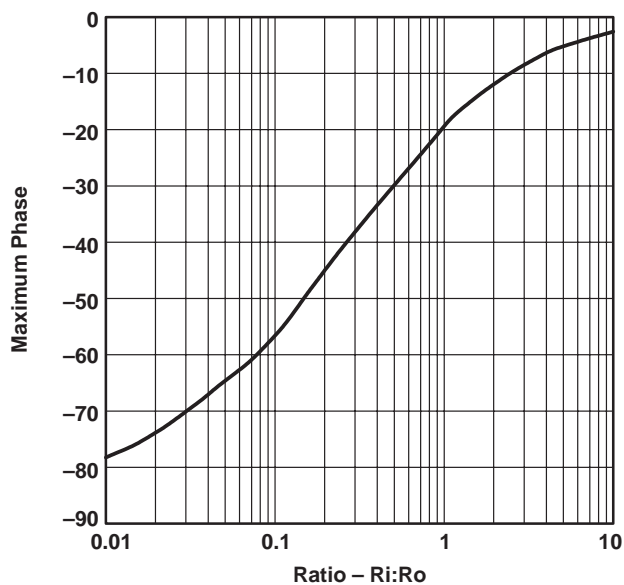


Figure 20. Maximum Phase Shift in $\frac{V_{fb}}{aV_e}$ vs the Ratio $R_i:R_o$

Figure 21 shows simulation results with the same circuits as used for Figure 16 ($R_o = 100 \Omega$ and $C_o = 159 \mu F$), but with $R_i = 100 \Omega$ added to the circuit. The circuits are stable.

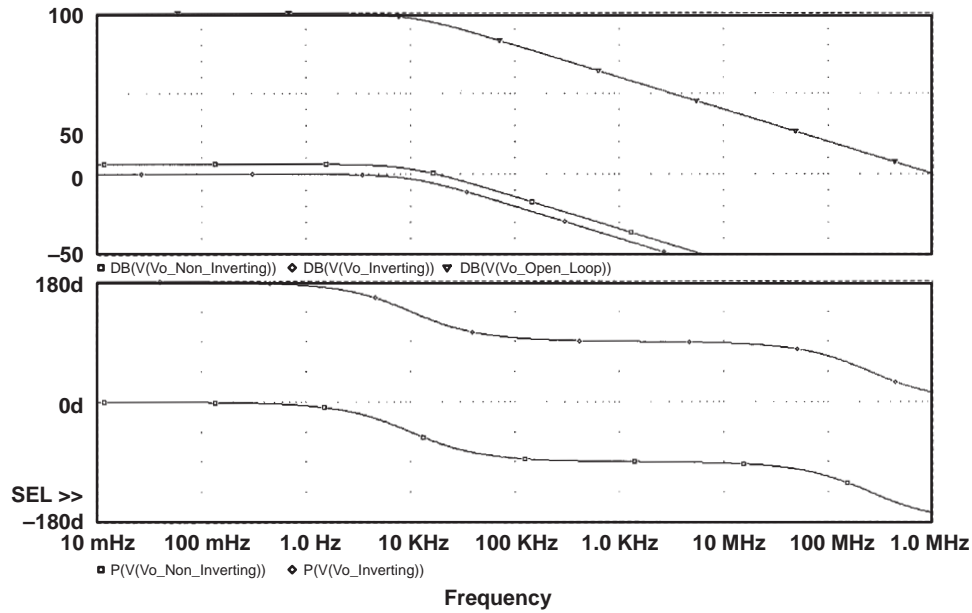


Figure 21. Spice Simulation Results with R_i Added to Compensate for R_o and C_o

A common use of an isolation resistor is shown in Figure 22 where a video buffer circuit is drawn. To avoid line reflections, the signal is delivered to the transmission line through a $75\text{-}\Omega$ resistor, and the transmission line is terminated at the far end with a $75\text{-}\Omega$ resistor. To compensate for the voltage divider, the gain of the op amp is 2.

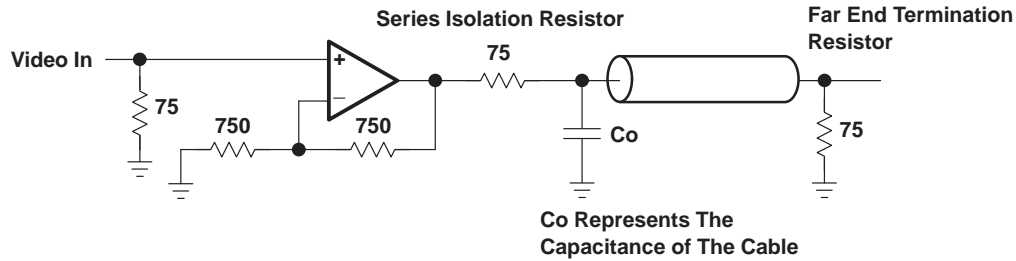


Figure 22. Video Buffer Application

If the load is unknown or dynamic in nature, method 3 is not satisfactory. Then method 4, the configuration shown in Figure 23, is used with better results. At low frequencies, the impedance of C_c is high in comparison with R_2 , and the feedback path is primarily from V_o restoring the dc and low frequency response. At higher frequencies, the impedance of C_c is low compared with R_2 , and the feedback path is primarily from V_{fb} , where the phase shift, due to C_o , is buffered by R_i .

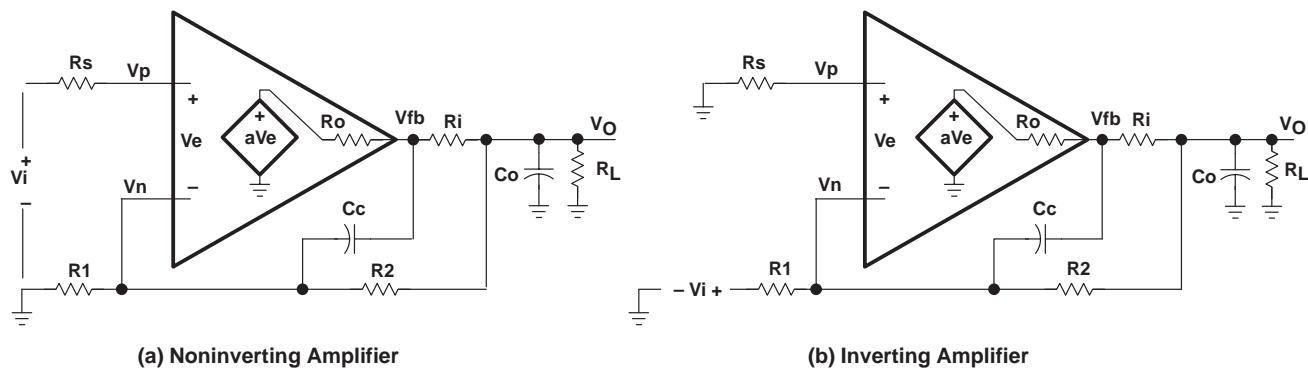


Figure 23. R_i and C_c Added to Compensate for Effects of R_o and C_o

To solve these circuits analytically is quite cumbersome. By making some simplifications, the basic operation is more easily seen. The transfer function of interest is $\frac{V_n}{aV_e}$.

Assume the impedance of R_1 and R_2 is much higher than the impedance of R_i , R_o and C_o , and $C_c \ll C_o$. At low frequencies, C_c looks like an open and the circuit can be represented as shown in Figure 24 (a). At higher frequencies C_c becomes active, C_o is essentially a short, and the circuit can be represented as shown in Figure 24 (b).

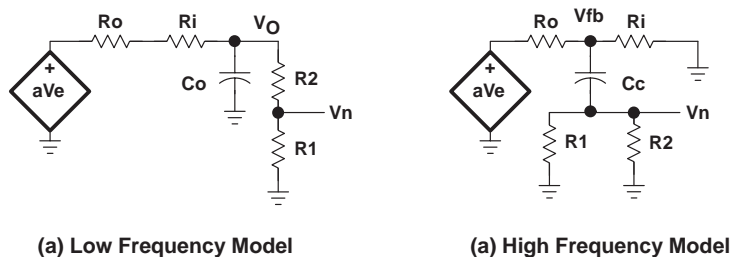


Figure 24. Simplified Feedback Models

This breaks the feedback into low and high frequency circuits:

$$\text{At low frequency: } \frac{V_n}{aV_e}(f_{low}) = \left(\frac{R_1}{R_1 + R_2} \right) \left(\frac{1}{1 + sC_o(R_o + R_i)} \right).$$

$$\text{At high frequency: } \frac{V_n}{aV_e}(f_{high}) = \left(\frac{R_i}{R_i + R_o} \right) \left[\frac{1}{1 + \frac{1}{sC_c(R_1 || R_2)}} \right].$$

The overall feedback factor is a combination of the two so that:

$$\frac{V_n}{aV_e} = \left(\frac{R_1}{R_1 + R_2} \right) \left(\frac{1}{1 + sC_o(R_o + R_i)} \right) + \left(\frac{R_i}{R_i + R_o} \right) \left[\frac{1}{1 + \frac{1}{sC_c(R_o + R_i)}} \right]$$

This formula contains a pole and a zero. Choosing the value of the components so that the pole and zero are at the same frequency by setting $C_c = C_o \frac{R_o + R_i}{R_1 || R_2}$ results in the feedback path switching from V_o to V_{fb} as the phase shift due to $C_o(R_i + R_o)$ transitions to -90° .

Figure 24 shows the simulation results of adding $C_c = 636$ nF with isolation resistor, $R_i = 100 \Omega$, to the feedback path (as indicated in Figure 23). The circuit is no longer unstable and the low frequency load independence of the output is restored. Simulation of the circuit shows similar results as those depicted in Figure 21, and is not shown.

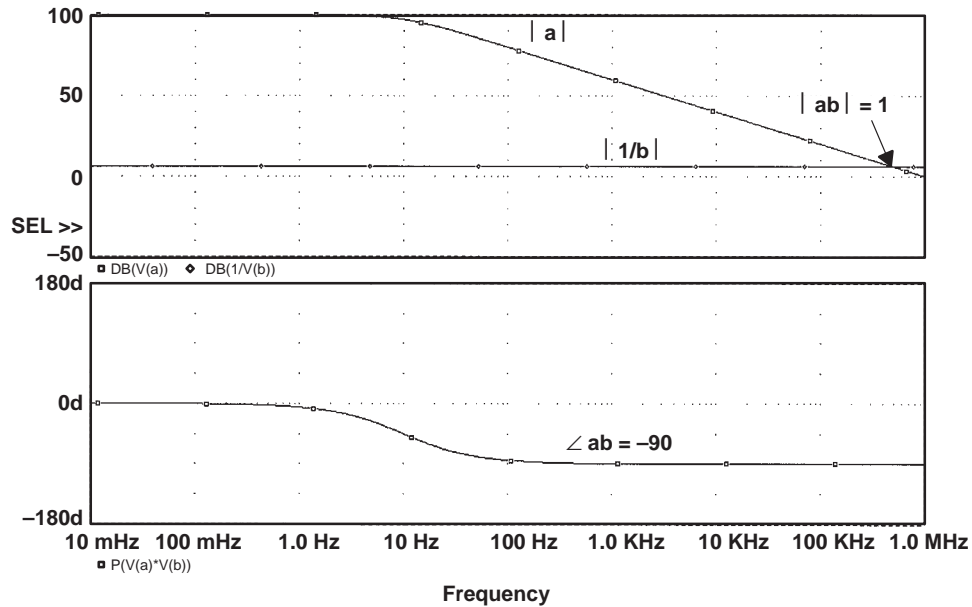


Figure 25. Simulation of Feedback Using R_i and C_c to Compensate for R_o and C_o

7 Summary

The techniques described herein show means for analyzing and compensating for known component values. In circuit application, the value of parasitic components is not always known. Thus the ubiquitous rule of thumb comes into play:

1. Always connect a small, 20-pF to 100-pF, capacitor between the output and the negative input.
2. If the op amp has to drive a significant capacitance, isolate the output with a small, 20-Ω to 100-Ω, resistor.

Table 1. Noninverting Amplifier: Capacitor Location, Effect, and Compensation Summary

Topology: Noninverting Amplifier		
Capacitor Location	Effect	Compensation
All places	Various	Reduce capacitance and/or associated resistance.
Negative input, C_n	Gain peaking or oscillation	Compensate with $C_2 = C_n \frac{R_1}{R_2}$ across R_2 .
Positive input, C_p	Reduced Bandwidth	Compensate with $C_1 \gg C_n$ across R_1 .
Output, C_o	Gain peaking or oscillation	<ol style="list-style-type: none"> 1. If load is known, isolate with resistor, $R_i = R_o$. This causes load dependence. 2. If load is unknown, isolate with resistor, $R_i = R_o$ and provide ac feedback from isolated point with $C_c = C_o \frac{R_o + R_i}{R_1 R_2}$. Provide dc feedback from V_o.

Table 2. Inverting Amplifier: Capacitor Location, Effect, and Compensation Summary

Topology: Inverting Amplifier		
Capacitor Location	Effect	Compensation
All places	Various	Reduce capacitance and/or associated resistance.
Negative input, C_n	Gain peaking or oscillation	Compensate with $C_2 = C_n \frac{R_1}{R_2}$ across R_2 , and $C_1 = C_n$ across R_1 .
Positive input, C_p	None	None
Output, C_o	Gain peaking or oscillation	<ol style="list-style-type: none"> 1. If load is known, isolate with resistor, $R_i = R_o$. This causes load dependence. 2. If load is unknown, isolate with resistor, $R_i = R_o$ and provide ac feedback from isolated point with $C_c = C_o \frac{R_o + R_i}{R_1 R_2}$. Provide dc feedback from V_o.

8 References

1. Paul R. Gray and Robert G. Meyer. *Analysis and Design of Analog Integrated Circuits*. 2d ed., John Wiley & sons, Inc., 1984.
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